A Research on a Double Auxiliary Resonant Commutated Pole Soft-Switching Inverter

Liang Huang, Enhui Chu, and Xing Zhang

***Abstract*—Aiming at overcoming the problem that the auxiliary switches in an improved auxiliary resonant communicated pole inverter may not realize zero-voltage turning off in practical application if there are parasitic inductors in the wiring process, this paper proposes a novel double auxiliary resonant commutated pole inverter. In novel topology, auxiliary capacitance and auxiliary switch are in parallel. This structure avoids the influence of parasitic inductors in the wire, and ensures the auxiliary switch to realize zero-voltage turning off reliably. The novel topology not only inherits all advantages of the improved auxiliary resonant communicated pole inverter, but also improves its reliability. Therefore the novel topology is more suitable for high power occasion.**

***Index Terms*—Soft switching, double auxiliary resonant commutated pole inverter, parasitic inductance, reliability.**

I. Introduction

In recent years, with the development of power electronics technology, the applications of soft-switching technology play an important role in high-frequency PWM inverters [1]-[4]. Among many inverter topologies, the auxiliary resonant inverter is an important type, which mainly includes resonant DC link inverters [5], resonant AC link inverters [6] and auxiliary resonant commutated pole inverters. Auxiliary resonant commutated pole inverters do not increase voltage and current stress of main switches, so they are more suitable for high-power occasions.

The traditional active auxiliary resonant commutated pole (ARCP) inverter [7] has two bulk capacitors, and the electric potential in neutral point is variable. Moreover, it need separate detecting circuits and logic control circuits, which lead to control circuits are very complicated. Although many improved ARCP inverters [8]-[11] solve the two bulk capacitors problem subsequently, they need either complex coupled inductors or transformers with corresponding magnetic flux reset circuits. Furthermore, the three single-phase resonant circuits of some inverters are coupled with each other. In addition, in order to achieve soft switching, some topologies also need additional detecting circuits and peripheral logic circuits. So the main circuit and control circuits will be very complicated.

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Then, an improved ARCP inverter with the function of pulse current regeneration is proposed in reference [12]. This topology not only avoids using two bulk capacitors, but also eliminates the neutral point potential variation. In addition, the three single-phase auxiliary commutation circuits in this topology are independent of each other, and they can be applied various modulation strategies easily. However, when considering the presence of parasitic inductors in the wiring process, there may be voltage spikes during the auxiliary switches turn off. So, the auxiliary switch cannot realize zero-voltage turning off reliably. The reliability of this topology is low.

To solve this problem, this paper proposes a novel topology with double auxiliary resonant commutated pole. By using the method of the auxiliary capacitor paralleling with the auxiliary switch directly, it is avoided that the influence of parasitic inductors in the wire. The novel topology not only inherits all advantages of the topology proposed in reference [12], but also assures that the auxiliary switch can realize zero-voltage turning off reliably when considering the presence of parasitic inductors in the wiring process. So the reliability of novel topology will be improved significantly.

II. Topology and Modulation Strategy

The novel topology is shown in Fig. 1. Since the structures of three single-phase auxiliary resonant circuits are identical and independent, they can be modulated by themselves. So one phase leg of the inverter is analyzed in this paper.

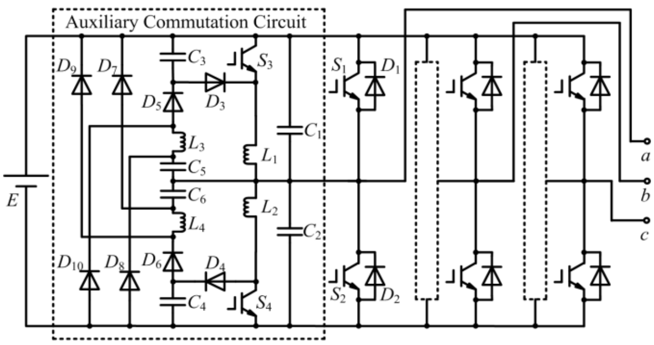

Fig. 1. The novel topology.

The auxiliary commutation circuit of the inverter is composed of auxiliary switches (S_3, S_4), main resonant capacitors (C_1, C_2), first resonant capacitors (C_3, C_4), second resonant capacitors (C_5, C_6), first resonant capacitors (L_1, L_2), second resonant capacitors (L_3, L_4), resonant diodes (D_3, D_4), (D_5, D_6), (D_7, D_8), (D_9, D_{10}). During the turn-on period of main switch S_1 (S_2), the voltage across main resonant capacitor C_1 (C_2) is zero. When main switch S_1 (S_2) is turned

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off, main resonant capacitors C_1, C_2 and first auxiliary resonant capacitor C_3 (C_4) will limit the voltage change rate of main switch S_1 (S_2) and provide zero-voltage-switching (ZVS) turn-off condition to S_1 (S_2). When auxiliary switch S_4 (S_3) is turned on, the current through first auxiliary resonant inductor L_2 (L_1) increases from zero and the auxiliary switch S_4 (S_3) realizes zero-current-switching (ZCS) turning on. When auxiliary switch S_3 (S_4) is turned off, the voltage across second auxiliary resonant capacitor C_5 (C_6) increases from zero and the auxiliary switch S_3 (S_4) realizes ZVS turning off. Besides, the energy stored in auxiliary resonant inductor L_1 (L_2) begins to transform to the auxiliary resonant capacitor C_3 (C_4). Until the voltage across first auxiliary resonant capacitor C_3 (C_4) is charged to input DC voltage E, the residual energy stored in the first auxiliary resonant inductor L_1 (L_2) is fed back to DC power supply by the energy regeneration feedback diode D_9 (D_{10}).

The modulation strategy is shown in Fig. 2. In sine-wave triangular-comparison pulse width modulation (PWM) with dead time, the operation sequence is designed as the on and off periods of main switches, which are alternated at intervals of π. The dead time is δ_{t1}. At the moment of turning off main switch S_1 (S_2), turn on auxiliary switch S_4 (S_3) immediately. Since the moment of turning on main switch S_2 (S_1), it is prolonged for δ_{t2}, and then turn on auxiliary switch S_4 (S_3).

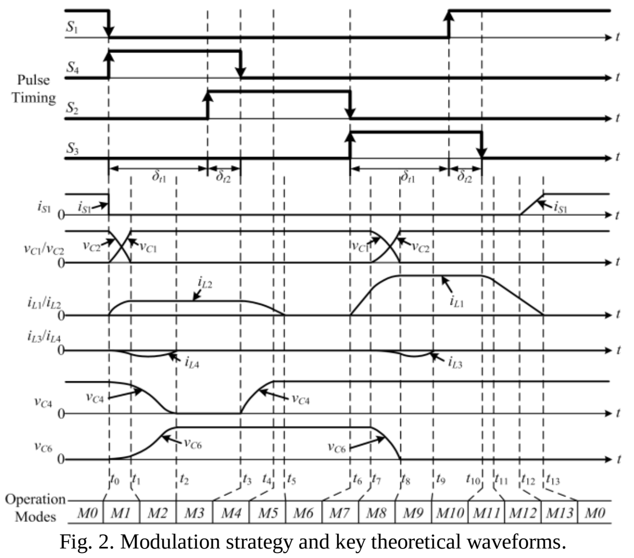

Fig. 2. Modulation strategy and key theoretical waveforms.

III. Operational Principle

In order to facilitate the analysis, several assumptions are employed:

1) All switches, diodes, capacitors and inductors are ideal devices.
2) The values of main resonant capacitors (C_1, C_2) are C_1=C_2=C_a. The values of first auxiliary resonant capacitors (C_3, C_4) are C_3=C_4=C_b. The values of second auxiliary resonant capacitors (C_5, C_6) are C_5=C_6=C_c. The values of first auxiliary resonant inductors (L_1, L_2) are L_1=L_2=L_a. The values of second auxiliary resonant inductors (L_3, L_4) are L_3=L_4=L_b.
3) Since the switching frequency f_s is much larger than the output current/voltage frequency f_o, the load current I_a is constant during one commutation processes. The reference positive direction of the load current is the same as the direction of the arrow in Fig. 3.

The key theoretical waveforms of novel topology are shown in Fig. 2, and the equivalent circuits of different operation modes are shown in Fig. 3.

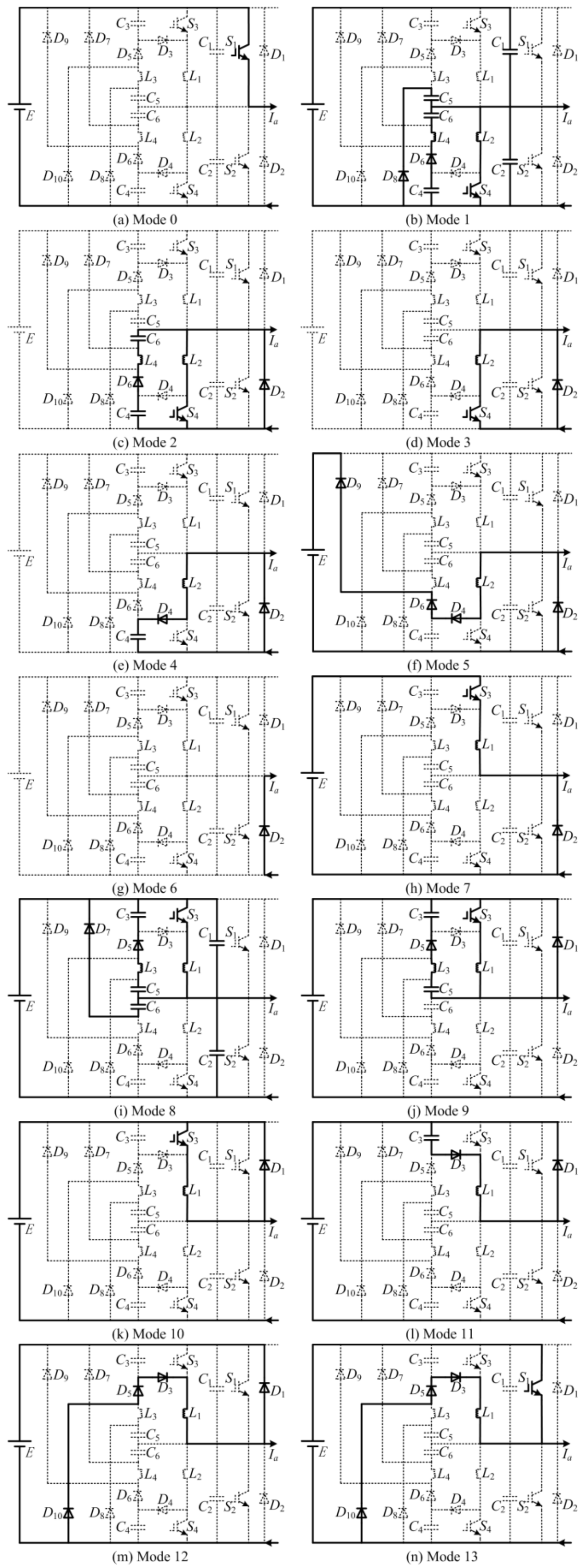

Fig. 3. Single-phase equivalent circuits of different operation modes

The operation modes are analyzed in detail as follows:

Mode 0 [~t_0]: Before t_0, S_1 is in the turn-on state and S_2, S_3, S_4 are in the turn-off state. This mode is the stable state that S_1 carries load current. Where v_{C1}=v_{C6}=0, v_{C2}=v_{C3}=E, v_{C4}=v_{C5}=E, i_{S1}= I_a.

Mode 1 [t_0, t_1]: At instant t_0, S_1 is turned off and the load current I_a is commutated to C_1, C_2 and C_5 immediately. C_1, C_2, C_5 and L_2 begin to resonate. The voltages across C_2 and C_5 fall from E. The voltage across C_1 rises from zero. S_1 is ZVS turn-off. The current through L_2 rises from zero. S_4 is ZCS turn-on. At the same time, C_4, C_6 and L_4 begin to resonate. The voltage across C_4 falls from E. The voltage across C_6 rises from zero. When the voltage across C_1 rises to E, mode 1 ends.

Mode 2 [t_1, t_2]: At instant t_1, the current through L_2 reaches to the maximum value i_{L2max}. The voltage across C_1 is charged to E and the voltages across C_2 and C_5 are discharged to zero. Diode D_8 turns off naturally. Diode D_2 starts conducting and the load current I_a is commutated to D_2 immediately. C_4, C_6 and L_4 continue to resonate. The voltage across C_4 falls down and the voltage across C_6 rises up. Because the voltage across L_2 is zero and invariable, the current through L_2 (i_{L2max}) is invariable during this mode. When the current through L_4 falls to zero, mode 2 ends.

Mode 3 [t_2, t_3]: At instant t_2, the voltage across C_4 falls to zero, and the voltage across C_6 rises to E. Diode D_6 turns off naturally. The resonant current flows through the series circuit (L_2-S_4-D_2). The current through L_2 (i_{L2max}) is invariable. If S_2 is turned on during this mode, it is ZVS turn-on. When S_4 is turned off, mode 3 ends.

Mode 4 [t_3, t_4]: At instant t_3, S_4 is turned off. L_2 and C_4 begin to resonant. The voltage across C_4 rises from zero. S_4 is a ZVS turn-off. When the voltage across C_4 rises to E, mode 4 ends.

Mode 5 [t_4, t_5]: At instant t_4, the voltage across C_4 rises to E. Diode D_8 and D_9 start conducting. The residual energy stored in L_2 is feedback to the input DC power supply through D_4, D_8 and D_9. When the current through L_2 falls to zero, mode 5 ends.

Mode 6 [t_5, t_6]: At instant t_5, the current through L_2 falls to zero, the load current I_a flows through D_2 and the value of I_a is invariable.

Mode 7 [t_6, t_7]: At instant t_6, S_3 is turned on. Since D_2 is conducting, the voltage across L_1 is E. So the current through L_1 rises linearly from zero. At the same time, the current through D_2 falls linearly from I_a. The load current I_a is commutated from D_2 to L_1 gradually. After S_3 is turned on, the current through L_1 rises from zero and S_3 is ZCS turn-on. When the current through L_1 reaches to I_a, the current through D_2 falls to zero. D_2 turns off naturally and mode 7 ends.

Mode 8 [t_7, t_8]: At instant t_7, D_2 turns off, and C_1, C_2, C_6 and L_1 begin to resonant. The voltages across C_1 and C_6 fall from E. The voltage across C_2 rises from zero. The current through L_2 rises from zero. At the same time, C_3, C_5, and L_3 begin to resonate. The voltage across C_3 falls from E. The voltage across C_5 rises from zero. When the voltage across C_2 rises to E, mode 8 ends.

Mode 9 [t_8, t_9]: At instant t_8, the current through L_1 reaches to the maximum value i_{L1max}. The voltage across C_2 is charged to E and the voltages across C_1 and C_6 are discharged to zero. Diode D_1 start conducting and the load current I_a is commutated to D_1 immediately. C_3, C_5 and L_3 continue to resonate. The voltage across C_3 falls and the voltage across C_5 rises. Because the voltage across L_1 is invariable, the current through L_1 is i_{L1max} and invariable during this mode. When the current through L_3 falls to zero, mode 9 ends.

Mode 10 [t_9, t_{10}]: At instant t_9, the voltage across C_3 falls to zero, and the voltage across C_5 rises to E. Diode D_5 turns off naturally. The resonant current flows through the series circuit (L_1-S_3-D_1). The current through L_1 (i_{L1max}) is invariable. If S_1 is turned on during this mode, it is ZVS turn-on. When S_3 is turned off, mode 10 ends.

Mode 11 [t_{10}, t_{11}]: At instant t_{10}, S_3 is turned off. L_1 and C_3 begin to resonant. The voltage across C_3 rises from zero. S_3 is ZVS turn-off. When the voltage across C_3 rises to E, mode 11 ends.

Mode 12 [t_{11}, t_{12}]: At instant t_{11}, the voltage across C_3 rises to E. Diode D_5 and D_{10} start conducting. The residual energy stored in L_1 is feedback to the input DC power supply E through D_3, D_5 and D_{10}. When the current through L_1 falls to I_a, mode 12 ends.

Mode 13 [t_{12}, t_{13}]: At instant t_{12}, the current through L_1 falls linearly to I_a. Diode D_1 turns off naturally. The current through S_1 rises linearly from zero. The load current I_a is commutated from L_1 to S_1 gradually. When the current through L_1 falls to zero, mode 13 ends. At the end of this mode, a switching cycle is achieved.

On the basis of the analysis mentioned above, in mode 4 (mode 11), because the first auxiliary capacitor C_4 (C_3) is parallel with the auxiliary switch S_4 (S_3) directly, the auxiliary switch can realize ZVS turn-off reliably. Especially when there are parasitic inductors in the wiring process, due to the presence of the auxiliary capacitor, the process of auxiliary switch turning off will not be affected.

However, for the topology in reference [12], the auxiliary switch is not parallel with a capacitor. So the auxiliary switch just realizes ZVS turn-off condition through mathematical methods according to Kirchhoff's voltage law. The equations will be not right, if there are parasitic inductors in the wiring process. So, the voltage across S_4 (S_3) is not equal to that across C_4 (C_3). Therefore, it is not sure that the voltage across S_4 (S_3) rises from zero. S_4 (S_3) does not realize ZVS turning off. Moreover, there are voltage spikes probably when S_4 (S_3) is turned off. The reliability cannot be assured.

IV. Simulation and Evaluation

The parameters of simulation are shown below. The nominal of output power is 1.8kW and the nominal of output line voltage is 50V. The output frequency is 50Hz and the switching frequency is 16kHz. The input DC voltage is 100V. The value of main resonant capacitor (C_1, C_2) is 100nF, the value of first auxiliary resonant capacitor (C_3, C_4) is 50nF and the value of second auxiliary resonant capacitor (C_5, C_6) is 50nF. The value of first auxiliary resonant inductor (L_1, L_2) is 2μH. The value of second auxiliary resonant inductor (L_3, L_4) is 20μH. The delay time δ_{t1} is 4μs, and δ_{t2} is 0.5μs. The simulation results are shown in Fig. 4.

Fig. 4 (a) shows the wave forms of current and voltage at the moment of turning off the main switch S_1 and the main switch S_1 achieves ZVS turning off. Fig. 4 (b) shows the wave forms of current and voltage at the moment of turning on the main switch S_1 and the main switch S_1 achieves ZCZVS turning on. Fig. 4 (c) shows the wave forms of current and voltage at the moment of turning on the auxiliary switch S_3 and the auxiliary switch S_3 achieves ZCS turning on. Fig. 4 (d) shows the wave forms of current and voltage at the moment of turning off the auxiliary switch S_3 and the auxiliary switch S_3 achieves ZVS turning off. Fig. 4 (e) shows the wave forms of current and voltage at the moment of turning on the auxiliary switch S_4 and the auxiliary switch S_4 achieves ZCS turning on. Fig. 4 (f) shows the wave forms of current and voltage at the moment of turning off the auxiliary switch S_3 and the auxiliary switch S_3 achieves ZVS turning off.

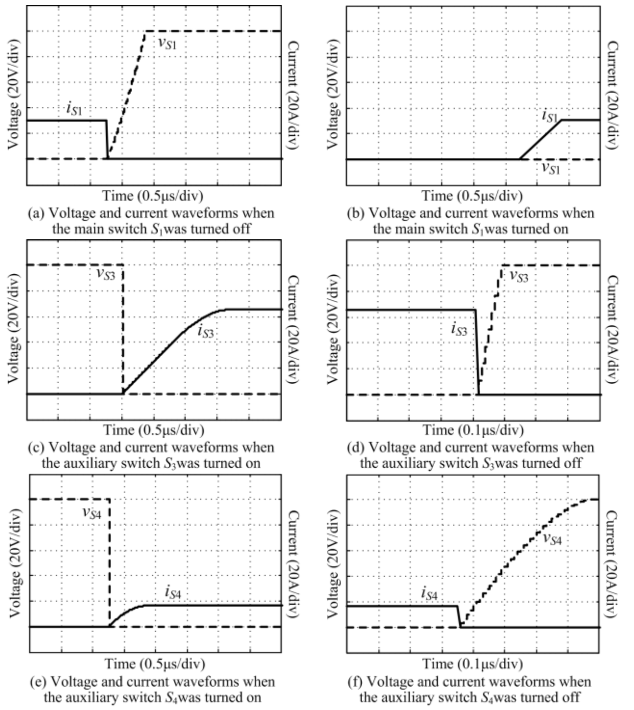

Fig. 4. Switching waveforms of the main switch S_1 and auxiliary switch S_3 and S_4

V. Conclusion

This paper proposes a novel topology. Through the theoretical analysis and simulation results, several conclusions have been got as below:

1) The detecting circuits and logic control circuits are not necessary and all main switches and auxiliary switches can realize ZVS or ZCS turning on and turning off. This is beneficial to increase the switching frequency.
2) The voltage stresses of devices are limited to no more than the input DC voltage E. This is beneficial to select devices.
3) The energy in auxiliary circuit can feed back to the input DC power supply. This is beneficial to improve the energy conversion efficiency.
4) The three single-phase auxiliary commutation circuits are independent of each other, and they can be applied various modulation strategies easily.
5) It is assured that both the main switch and the auxiliary switch can realize ZVS turning off reliably, when there are parasitic inductors in the wiring process in practical application. So the reliability will be improved significantly.

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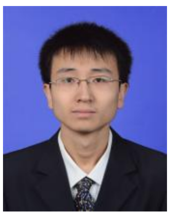

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