Design and Analysis of a Low Power UWB Pulse Generators

Saleh M. Eisa, Hanady H. Issa, Khaled A. Shehata, and Hani F. Ragai

***Abstract*—This paper presents three configurations of Ultra Wideband (UWB) Pulse Generators (PGs). The Generators target low power applications operating in the frequency range 3.1-10.6 GHz. The designs use logic gates and buffered filters to generate a Gaussian 5th derivative pulse. The used technology is 0.13 µm from TSMC. The lowest power consumption and highest BW achieved are 0.13 mW and 7.1 GHz respectively. In terms of Power Spectral Density (PSD), the designs comply with the -41.3 dBm FCC requirements.**

***Index Terms*—Ultra wideband, pulse generators, gaussian pulse, ring oscillator.**

I. Introduction

Signals having a Bandwidth (BW) of 500 MHz or a Fractional Bandwidth (BWf) less than or equal to 0.2 are considered as UWB signals according to the Federal Communications Commission (FCC) definition [1]. In order for UWB applications to coexist with common wireless communication systems without any interference, the FCC has defined PSD masks for different applications. Indoor UWB applications have an allocated bandwidth that extends from 3.1 to 10.6 GHz with a maximum PSD of -41.3 dBm. This PSD level represents the unintentional power radiated from television sets or monitors. UWB signals are characterized by short pulses with duration less than 1 nsec, relatively low power and wide BW. These characteristics migrate UWB from military applications towards commercial applications. Because of its wide BW, UWB signals are suitable for high data rate applications over short distances (several meters) such as wireless Personal Area Networks (WPAN) [2]. UWB can even be used for shorter distance applications such as Body Area Networks (BAN) [3]. Besides, high data rates UWB signals can also be used for low data rate with higher range as in Wireless Sensor Networks (WSN) [4] and Radio Frequency Identification (RFID) applications [5].

II. UWB Pulse Generation

The Pulse Generator (PG) is the most important part of the UWB system. Design simplicity is the most attractive aspect of UWB PGs when compared to common communication systems. Different pulse shapes such as rectangular, cosine and Gaussian pulses are used for UWB communications. Among all, the Gaussian pulse is the most common used because of its ease in generation. In addition, Gaussian pulse has a smooth transition in time domain and better frequency response. Step Recovery Diodes (SRD) and avalanche transistors are employed to generate Gaussian pulses [6], [7]. Logic gates are also used to generate Gaussian pulses [8]. To comply with the FCC requirements, pulse shaping filters are used to transform the generated pulse to a higher order derivatives Gaussian pulse [9].

This paper proposes three different UWB PGs. The core of the proposed PGs is the ring oscillator. The generated pulse is then shaped to produce a Gaussian 5th derivative pulse that complies with FCC regulations. The shaped pulse has duration less than 1 nsec. The generated pulse occupies a frequency band from 3.1 to 10.6 GHz. The PGs are designed on TSMC 0.13 µm CMOS technology and 1.2 V voltage supply using Cadence tools.

III. Design 1: Free Running 21-Stage Ring Oscillator UWB PG

The first PG design consists of a 21-stage ring oscillator, gated clock generator, Gaussian pulse generator, buffer circuit and a shaping filter module as shown in Fig. 1.

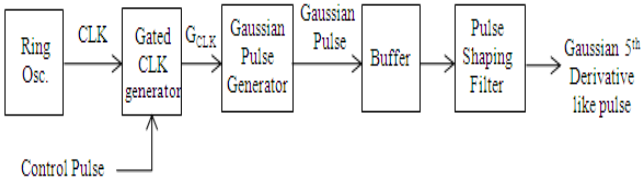

Fig. 1. First PG design.

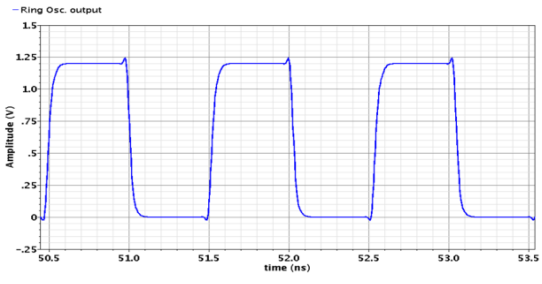

Fig. 2. Ring oscillator output.

The stages used in this oscillator utilize a minimum sized NMOS while the PMOS is designed to compensate the difference in mobility. A series of simulations are executed to determine the rise and fall time for the generated pulse associated with the oscillator. The number of inverter stages needed to produce a 1 nsec output signal is 21 stages. The simulated output of the designed ring oscillator is plotted in

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Fig. 2. An AND gate is used as a gated clock generator. The AND gate inputs are driven by the ring oscillator output and a 20 ns control pulse. The control pulse is used to adjust the overall bit rate of the system. The Gaussian Pulse is generated from a two-input NOR gate. One input is driven directly from the gated clock and the other is driven by a delayed one as shown in Fig. 3. The generated Gaussian pulse with a 250 psec width is shown in Fig. 4.

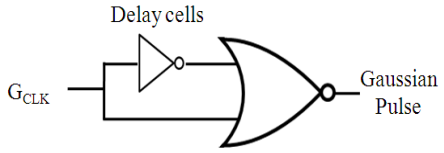

Fig. 3. The Gaussian pulse generator module.

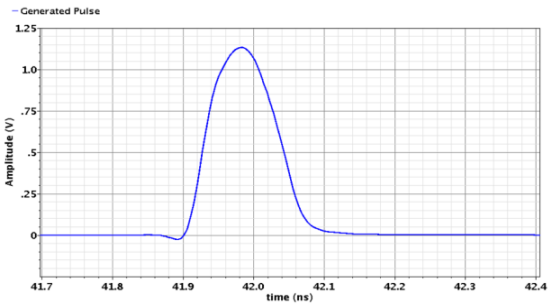

Fig. 4. The generated Gaussian pulse.

The pulse shaping filter in Fig. 1 is constructed using LC pi section 3rd order Butterworth Band Pass Filter (BPF). The filter type is chosen because it has the maximum flat response in its mid band [10]. The -10 dB bandwidth of the designed filter is 7.5 GHz. ADS tools are used in designing this filter. The equivalent input and output impedances of the filter are 50 Ω to match the buffer output and antenna load impedances. The S12 parameter of the BPF is plotted in Fig. 5. The filter response shows that the lower and upper -10dB cutoff frequency are 3.2 and 13 GHz respectively. Due to components degradation at high frequencies the upper cutoff frequency will comply with the FCC regulations.

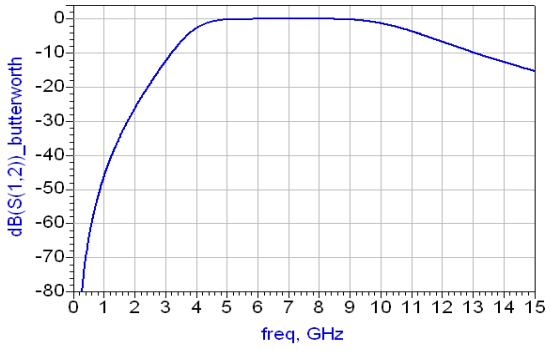

Fig. 5. S12 parameter of the Butterworth filter.

A buffer is utilized to separate the Gaussian Pulse Generator (GPG) circuit from the shaping filter. In addition, it is used to transform and match the GPG and load impedances for better filter response. The buffer consists of 6 stages with a stage ratio of 3 [11]. The first and last stages are designed to match the 11.2 kΩ output impedance of the GPG with the 50Ω input impedance of the filter. The generated pulse has 660 mV peak-to-peak amplitude and 590 psec pulse duration as shown in Fig. 6. The pulse BW extends from 3.1 to 10.2 GHZ with a maximum PSD of -41.5 dBm at 5.4 GHz as shown in Fig. 7.

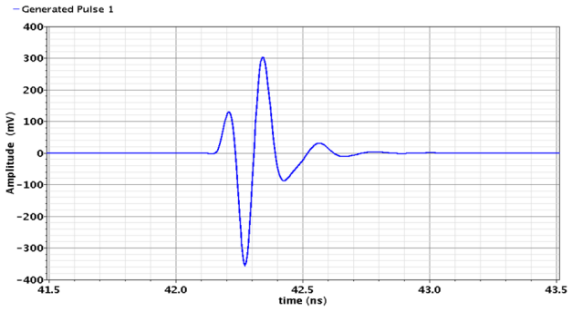

Fig. 6. Pulse generated from design 1.

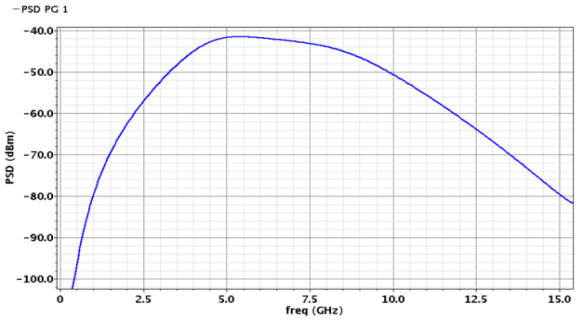

Fig. 7. PSD of generated signal in design 1.

IV. Design 2: A Controlled 21-Stage Ring Oscillator UWB PG.

The second PG design consists of a voltage controlled ring oscillator, a Gaussian pulse generator, buffer circuit and a pulse shaping filter as shown in Fig. 8. The controlled 21-stage ring oscillator is based on the same design presented in [9], [12]. An NMOS transistor is connected in series with the other 21 stages as shown in Fig. 9. In Addition, a PMOS transistor is inserted between the first two stages. The output pulse of the controlled oscillator is similar to the gated clock generated in design 1.

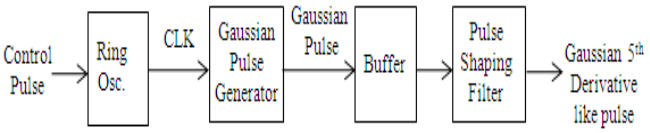

Fig. 8. Second PG design.

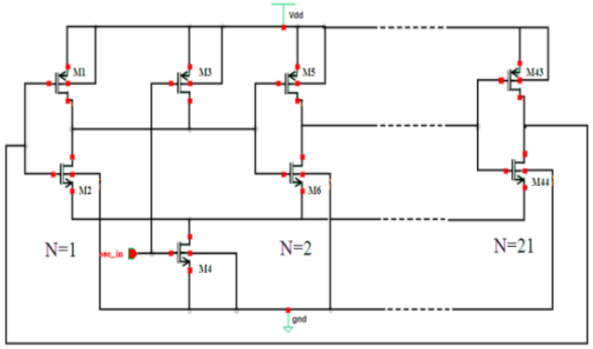

Fig. 9. A 21-Stage controlled ring oscillator.

A control signal is used to turn the added transistors ON/OFF and thus control the current pass to the ground.

When the control signal is high the added NMOS transistor is turned ON allowing the oscillator to run. When the control signal is low the output of the oscillator is pulled up to V_{DD} by the added PMOS. The same circuit for the Gaussian pulse generator, buffer circuit and shaping filter presented in the first design are utilized. The generated Gaussian 5th derivative pulse is presented in Fig. 10.

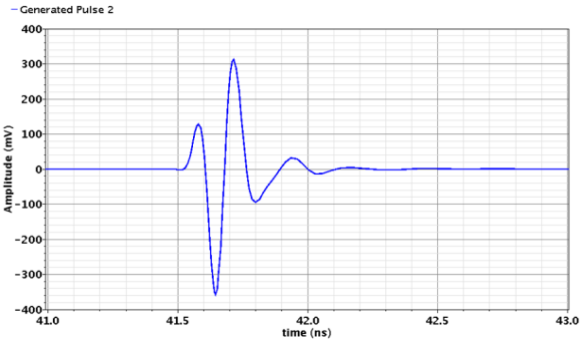

Fig. 10. Pulse generated from design 2.

The generated pulse has peak-to-peak amplitude of 670 mV and pulse width of 590 psec. The PSD shows that the generated pulse complies with FCC requirements as Fig. 11. The BW of the pulse is 7 GHz with lower and upper cutoff frequencies 3.1 and 10.1GHz respectively. The maximum simulated PSD is -41.3 dBm at 5.3 GHz.

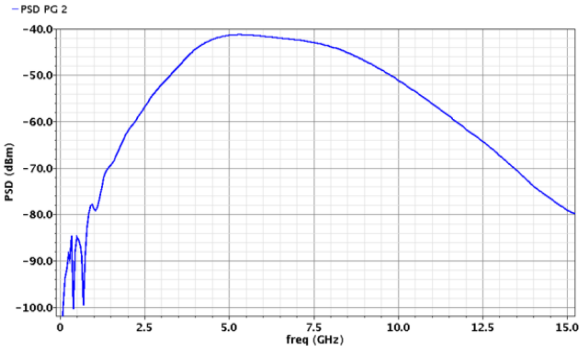

Fig. 11. PSD of generated signal in design 2.

V. Design 3: A Controlled 3-Stage Ring Oscillator UWB PG

In this design a 3-stage controlled ring oscillator is used. The design is based on the same idea presented in design 2 [9]. The block diagram for the pulse generator is shown in Fig. 12. The Control pulse switches the oscillator ON and OFF. The oscillator generates Gaussian pulse with 250 psec pulse duration. The peak-to-peak amplitude of the generated pulse is 690 mV with pulse width of 690 psec as shown in Fig. 13. The pulse has a maximum PSD of -41 dBm at 5.3 GHz as shown in Fig. 14. The BW of the pulse is 6.8 GHz with lower and upper cutoff frequencies of 3.1 and 9.9 GHz respectively.

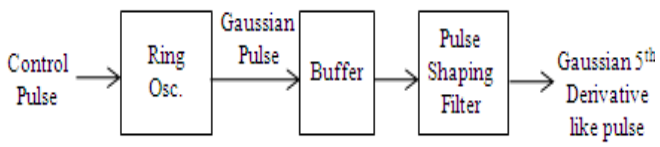

Fig. 12. Third PG design.

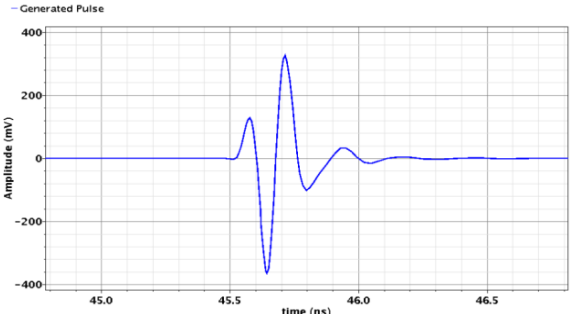

Fig. 13. Pulse generated from design 3.

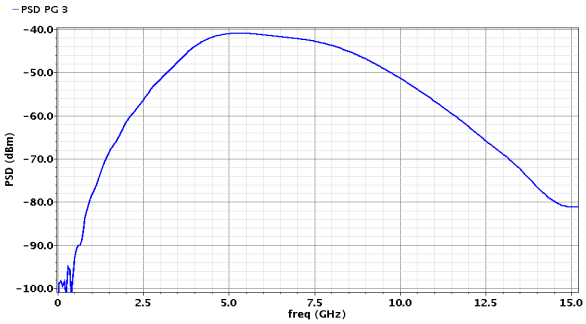

Fig. 14. PSD of generated signal in design 3.

VI. Simulation Results and Discussion

The buffering and shaping filter circuits are identical in the three designs. The only difference between the three designs is the method of generating the Gaussian pulse, mainly the ring oscillator. The total power dissipation, peak-to-peak amplitude, BW and the PSD are simulated. Table I shows that the three designs have comparable results in terms of BW and PSD. Design 3 has the highest output voltage while design 1 has the lowest voltage. Design 2 and 3 consume the same power while design 1 consumes 54 % more power. This can be attributed to the free running 21-stage ring oscillator.

TABLE I: Comparison Among the Three Designs

Pulse Generator	Generated Pulse			
	Total Pavr. (mW)	Amp. (mVp-p)	-10dB BW (GHz)	PSD (dBm)
Design 1	0.2	660	3.1-10.2	-41.5
Design 2	0.13	670	3.1-10.1	-41.3
Design 3	0.13	690	3.1 – 9.9	-41

VII. Conclusion

Three designs for UWB PGs are presented in this paper. The designs utilize ring oscillators with different number of stages to generate a Gaussian pulse. The pulse is then transformed to its 5th derivative using a Butterworth BPF filter. The Design containing a free running 21-stages ring oscillator consumes 0.2 mW which is the highest power consumption among the three designs. While the designs with the controlled ring oscillators consume 0.13 mW. The PSDs of the three designs vary from -41 to -41.5 dBm which satisfy the FCC requirement for indoor applications. The accomplished BWs range from 6.8 to 7.1 GHz satisfying the

UWB requirements.

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