# The Design of Platform System for Measuring Bio-Signal with Array Sensors

Donghoon Lee, Seungpyo Jung, Youngju Park, Sangman Kim, and Jusung Park

***Abstract*—Platform system for measuring the bio-signal, especially Aptamer using array sensor is designed. This platform system is based on 32-bit RISC processor, AMBA bus, peripheral device and interface for array sensors. Array sensors measure a variation of capacitance value by reaction with Aptamer from bio-signal. Processor reduces noise from measured bio-signal and carries out bio-signal processing algorithm.**

***Index Terms*—Bio-signal, micro-processor, platform system, processor.**

## I. Introduction

Aptamer from bio-signal can be a decision factor whether people have a disease. For example, Aptamer data of a liver cancer patient are different from non-cancer people. We gather Aptamer data of about 300 people, some of them have a liver cancer and the others are normal. If sensor measures this data, it can detect a minute capacitance change. Changing capacitance is a kind of analog signal of CMOS technology level. So if this signal is converted to digital, we can process it with many algorithms.

This paper suggests a platform system that measures bio-signal with array sensors and carries out signal processing algorithms. The platform system has RISC processor, AMBA bus, memory, peripheral device and GPIO for ADC with array sensor. And we design a test PCB board.

## II. Bio-Signal Processor

Sensor based on the CMOS technology transfers valid bio-signals. We design a bio-signal processor. For simple structure of processor core, it is based on RISC and it is suitable for mobile device because of low power. And 32-bit data depth is decided for accuracy of bio-signals. The processor can carry out calculation of signals, such as logical and arithmetic operation [1].

### A. Features

Processor has a 32-bit 3 stages pipeline structure, fetch, decode and execution. Execution cycle of every instructions and fetch cycle of next instruction are carried out at the same time [2].

And processor has 32-bit data bus and 32-bit address bus. For fast interrupt operation, processor has the fast interrupt function. Also it has simple but powerful instruction sets [3]-[4].

Manuscript received October 20, 2012; revised November 29, 2012.

Donghoon Lee, Seungpyo Jung, Youngju Park, Sangman Kim, and Jusung Park are with the Department of Electronic engineering, Pusan National University, Busan, Korea (e-mail: minuet21@pusan.ac.kr; spyam@pusan.ac.kr; pfhjh@pusan.ac.kr; kcoin@pusan.ac.kr; juspark@pusan.ac.kr)

### B. Architecture

The processor consists of many functional blocks shown as figure 1. It has the Multiply-Accumulator (MAC), 32-bit ALU, a barrel shifter and so on [1].

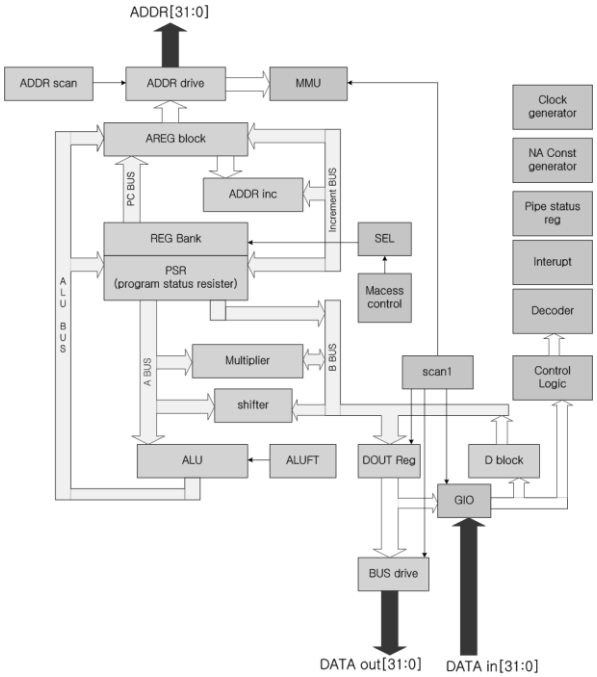


Fig. 1. Architecture of the processor

1) *ALU.* ALU can carry out 32-bit floating operations like addition and subtraction for one cycle. Two buses link register bank to ALU and provide input operand of ALU, third bus transfer results of ALU to register bank or address generating register.

2) *Multiplier*. Processor has internal multiplier can carry out 32x8 bit multiplication for one cycle under the early termination algorithm and modified Booth's algorithm. Also addition and multiplication are carried out for one cycle.

3) *Internal Bus.* Processor has 5 32-bit internal buses, increment bus, ALU bus, A bus, B bus and PC bus. Each bus connects to functional blocks such as register banks, ALU, barrel shifter, multiplier and address register. And PC data is stored to address register through PC bus.

4) *Register Bank.* Register bank has 31 32-bit general registers and 6 PSRs (program status register).

## III. Platform System

Bio-signal processor platform is designed with a

processor, array sensors, ADC and other peripheral device shown as figure 2.

### A. Architecture

Overall platform system consists of processor, OCD, external buses, LCD, memory blocks and array sensors with ADC. All of devices excluding sensors and ADC are designed with Verilog HDL (hardware description language) and are synthesizable.

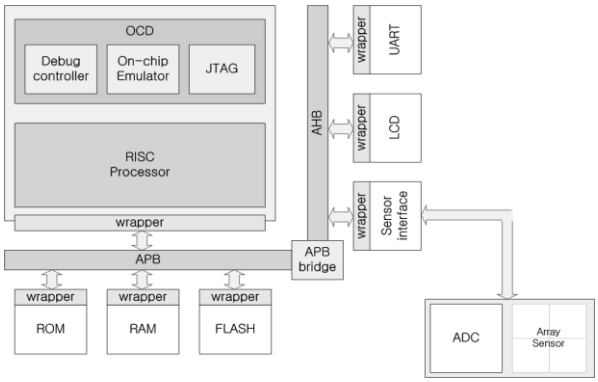


Fig. 2. Block diagram of platform system

Processor with OCD. OCD (on-chip debugger), logic can perform debugging functions embedded to the processor. Functions of OCD are five types, stopping a processor program execution, checking processor status, checking memory status, re-running processor program execution and real-time monitoring [5]-[8]. So user can check processor register or memory while processor carries out an application algorithm. If there is incorrect value in register, user stops execution of processor and modifies it with correct value. Then user re-runs an execution. OCD logic is very helpful when developing an application program such as filter algorithm and disease decision.

1) *External memory blocks.* Bio-signals from sensors are *stored* in RAM and they are inputted to ALU or internal memory block of the processor. Application programs are stored in ROM or flash. These codes are inputted to an instruction decode in the processor.

2) *External Bus.* Platform system uses AMBA (Advanced *Microcontroller* Bus Architecture architecture) to connect and control peripheral devices and memory blocks [9].

3) *UART.* Processor translates processed data to a computer using the UART. UART is commonly used in an integrated circuit, translates data with serial communication standard. Processor translates filtered or processed bio-signals to the *computer*, computer stores these data or displays an application program results to a monitor.

4) *LCD.* Processed bio-signals can be displayed at LCD *panel*. LCD shows measured signals from array sensor or status of array sensors.

### B. Array Sensor

Array sensor can measure a minute capacitance value, pF. If a bio-device can provide bio information such Aptamer, it reaches on surface of a sensor, a variety of capacitance is occurred. So we obtain these valid capacitance signals. Capacitance value is an analog data and based on CMOS technology, so it needs to change as digital data for bio-signal processing at the processor. Sensors are arranged as the 2x2 array and one ADC chip is used shown as figure 3.

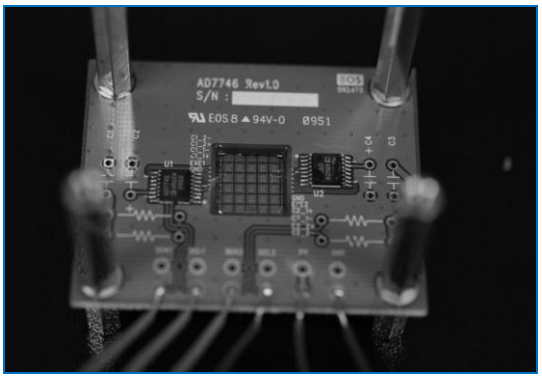


Fig. 3. Array sensors and ADC chip

### C. Sensor Interface

Processor translates data to sensors through external bus. Commercial ADC chip, AD7466 is used to connect between sensors and processor. This chip uses I2C (Inter-Integrated Circuit) communication protocol. So processor can control ADC chip and translate data to ADC using I2C protocol. Capacitance values measured at array sensors are inputted to ADC chip and ADC sends converted digital values to external bus. AD7746 provides a multi-channel input capacitance. The first stage, two channels, 2x2 array sensors, is designed. And I2C master core is designed using an open core controller.

## IV. Implementation and Verification

Suggesting bio-signal processor platform system must implement FPGA level to verify this system and design a portable system [10].

First of all, overall platform system is designed using HDL and synthesized under a FPGA level. Target FPGA chip is Xilinx Vertex-IV. This chip has more than 10k gates count, so it is enough to implement the platform system. After implementation of FPGA, PCB of this platform system is designed and implemented. Because a commercial FPGA board has many unnecessary peripheral devices and it is large.

### A. FPGA

Platform system, shown as figure 5, excluding ADC and sensor is synthesized and implemented to FPGA core. Also RTL level simulation of platform operation is carried out. Instruction set execution, application program execution, OCD logic performance and ADC with sensor interface must be verified [11]. Figure 4 shows an example of an instruction set simulation, INCODE. Platform system is verified its correct working through above simulations.

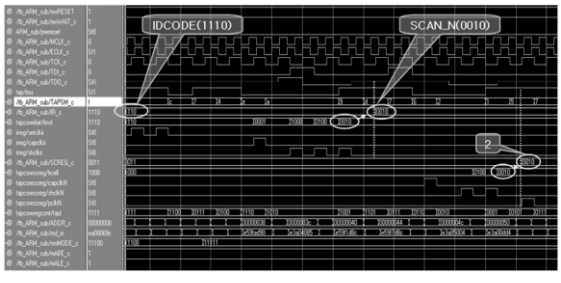


Fig. 4. Instruction simulation

### B. Platform Board

Suggesting platform system consists of 4 type components, processor, GPIO, LCD and peripheral devices. Its specifications are that, Xilinx Vertex-IV LX40 FPGA chip, SRAM 9Mb(256k x 36), FLASH 32Mb(128k x 32), 50Mhz system clock rates, UART & USB 2.0 PC interface, 320 x 240 pixels LCD panel, 60 pins GPIO, push buttons and LEDs.

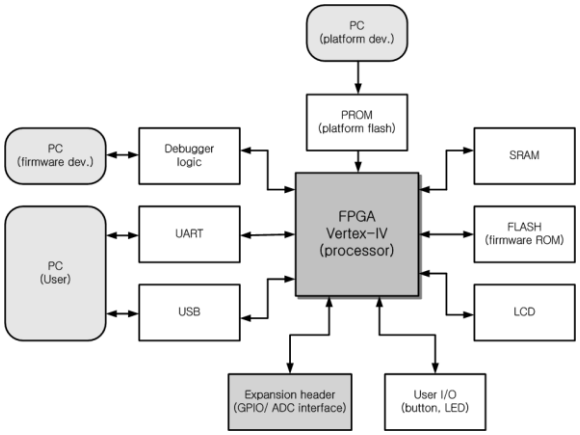


Fig. 5. Block diagram of platform board

Figure 5 shows signal flows between FPGA and IC devices. Downloading data to FPGA is translated to PC using JTAG and are stored at PROM and FLASH. FPGA controls external RAM and FLASH and translates data to PC using UART and USB. Also measured bio-signals from sensors are controlled by FPGA. ADC chip is connected to FPGA with GPIOs.

Bio-signals through GPIO may have much noise components. So a length between FPGA and GPIO is important for low noise signal when designing a circuit. Short length between them is better. Under this fact, a PCB is designed shown as Figure 6.

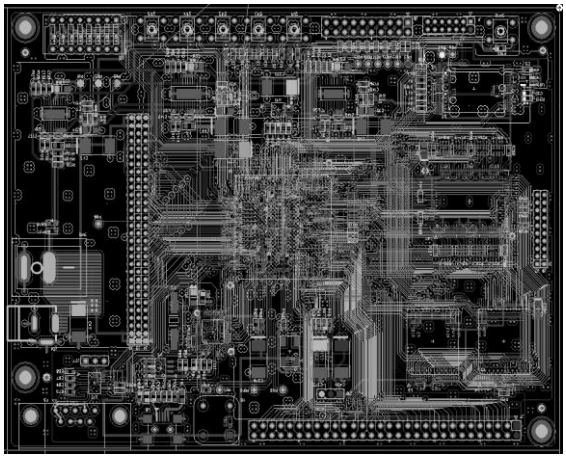

Fig. 6. Layout of platform board

A size of the bio-signal processor board can be reduced but a size of LCD daughter board above FPGA chip is fixed for a LCD panel. 320 x 240 pixels. This LCD panel is not designed by me, but a commercial board using LG panel.

An environment of board is shown as figure 7. A JTAG port on a board is connect to a computer for downloading a FPGA synthesis file and debugger JTAG port is connected to same computer for debugging and checking a process status. Also UART port translates data to a computer. The data are processed bio-signals.

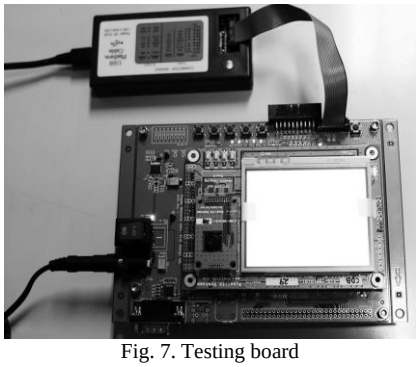

Fig. 7. Testing board

## V. Measurement and Processing Algorithm

Bio-signals measured on array sensors are inputted to the processor and processor carries out bio-signal processing and sends processed signal to LCD to display results or to computer.

### A. Bio-Signal Processing

Measured data on sensors are sensitive and low level capacitance value. Also these data can be added noise components generated in external factor. So bio-signals from ADC and sensors have much noise components. So processor excludes noise from measured data on sensors using a signal processing.

Throughout a low-pass filter, 150-orders FIR low-pass filter, reduced noise components signal can be obtained. Bio-signals measured on sensors have different properties by measuring matter or concentration. So each bio-signal has different sample data shown as figure 8. Black signal is 50 nM DNA and blue signal is 500 nM DNA. These signals are processed by a processor. A slope of each signal and their saturation values are different. By these properties, processor can analyze these signals and detect their status, normal or abnormal in real-time.

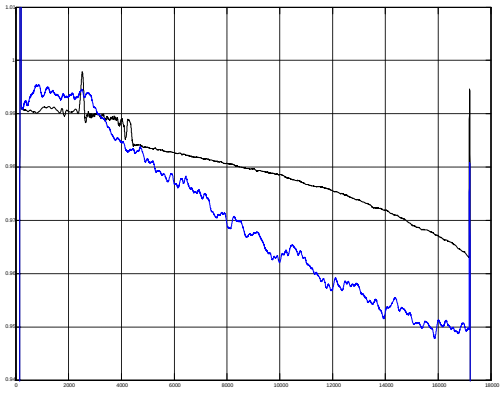

Fig. 8. Processed bio-signal

### B. LCD Display

Processed bio-signals show at LCD panel of a platform board. We design the LCD display procedure for maximum 2x2 array sensors shown as figure 14. Bio-signals are displayed on left and a measured sensor is displayed on right. When sensor measures bio-signal, we can check measured data in real-time. In a circle of a figure 9, processed

bio-signals are displayed. According amplitude of signals, a color is changed. If 2x2 array sensors measure bio-signals at the same time, four signals could be displayed on LCD.

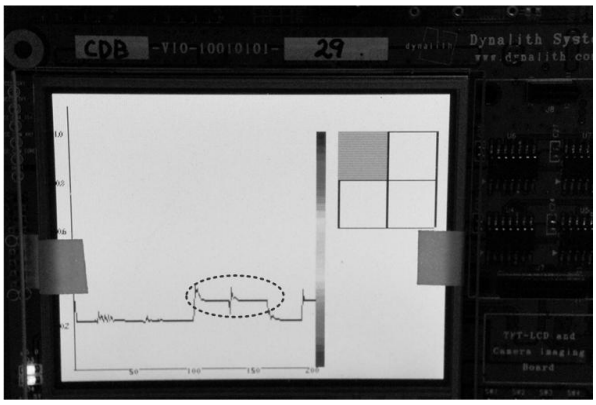

Fig. 9. LCD display

## VI. Conclusion

We design platform system for measuring bio-signal with array sensors. Array sensors measured a variation of capacitance from Aptamer. Processor carries out bio-signal processing algorithm with measured signal from sensors. Designed processor is synthesized and verified RTL level simulation. And we implement processor on FPGA and design test PCB board with bio-signal processing algorithm which reduces noisy from measured data and analyze bio-signals. Platform system consists of RISC processor, AMBA bus, peripheral devices, LCD for displaying measured and processed signal and GPIO for interface to ADC and array sensors.

## References


[1] S. Furber, *ARM System-On-chip Architecture*, Addison-Wesley, 1996.

[2] *ARM7TDMI Data sheet (ARM DDI 0029E)*, Advanced RISC Machines Ltd.(ARM), 1995.

[3] D. Jagger, *ARM Architecture Reference Manual*, Prentica Hall, London, 1996.

[4] D. Seal, *ARM architecture reference manual*, Addison-Wesley, 2001.

[5] H. Bleeker, P. V. D. Eijnden, and F. de Joun, *Boundary-Scan Test : A Practical Approach*, Kluwer Acadeemic Publishers, 1993.

[6] K. P. Parker, *The Boundary-Scan handbook*, Kluwer Academic Publishers, 2003.

[7] *IEEE Standard 1149.1-1990 IEEE Standard Test Access Port and Boundary-Scan Architecture*, (ANSI/IEEE), IEEE, Piscataway, NJ, 1990.

[8] J. Haufe, C. Fritsch, M. Gulbins, V. Luck, and P. Schwarz, "Real-Time Debugging of Digital Integrated Circuits," in *Proc. Design, Automation and Test in Europe Conf., User Forum*, Paris, March 27-30, 2000.

[9] *AMBA Specification (ARM IHI 0011A)*, ARM Ltd, 1999.

[10] A. S. Berger, *Embedded Systems Design: An Introduction to Processes, Tools and Techniques*, 2002

[11] T. Chang, "A Biased Random Instruction Generation Environment for Architectural Verification of Pipelined Processor," *J. of Electronic Testing*, 2000. pp. 13-27.


**Donghoon Lee** received B.S. and M.S. degrees in electronic engineering from Pusan National University, Busan, Korea, in 2005 and 2007, respectively. He is currently working toward a Ph.D. degree at the VLSI Design Laboratory, Department of Electronic Engineering, Pusan National University. His research interests include design of digital signal processor, design of multiprocessor SoC platform, and development of audio algorithm.

**Seungpyo Jung** received the B.S. and M.S. in electronic engineering from Pusan National University, Busan, Rep. of Korea, in 2007 and 2009, respectively. He is currently working toward the Ph.D. in electronics engineering at Pusan National University, Rep. of Korea. His research interests include microprocessor design and multimedia platform implementation.

**Youngju Park** received B.S. and M.S. degrees in electronic engineering from Pusan National University, Busan, Korea, in 2008 and 2010, respectively. He is currently working toward a Ph.D. degree at the VLSI Design Laboratory, Department of Electronic Engineering, Pusan National University. His research interests include design and verification methodology of digital blocks.

**Sangman Kim** received B.S. degrees in electronic engineering from Pusan National University, Busan, Korea, in 2011. He is currently working toward a M.S. degree at the VLSI Design Laboratory, Department of Electronic Engineering, Pusan National University. His research interests include design of multiprocessor SoC platform, and development of bio-signal processing.

**Jusung Park** was born in Junju, Korea, on 1953 December 19. He received a B.S degree in electronic engineering from Pusan National University, Busan, Korea, in 1976, an M.S. degree in electrical engineering from KAIST, Seoul, Korea, in 1978, and a Ph.D. degree in electrical engineering from the University of Florida, Gainsville, US, in 1989.
From 1978 to 1991 he was with ETRI, Daejun, Korea, as a principal research engineer, manger, and director of the IC design group. While at ETRI he designed several bipolar analog ICs and was in charge of developing VCR ICs, CMOS 8-bit microprocessors, and telecommunication chips. In 1991 he joined the Electronics Department of Pusan National University, Busan, Korea, where he is now a professor of electrical engineering. His current research interests are microprocessor and DSP core design, and digital audio algorithm implementation by hardware and software codesign.