Digital Multi-Bit Sigma-Delta Controller for Synchronous Buck DC-DC Converter

B. Abdi, *Member*, *IACSIT,* T. Moosazadeh, and J. S. Moghani

***Abstract*—A digital multi-bit sigma-delta controller is proposed to control a synchronous buck dc-dc converter over wide range of load currents and input voltages. A multi-bit sigma-delta modulator obtains the PWM control and makes the control loop. The output of the sigma-delta is used to control two paths power switches. An extra inductive path is used in parallel with main inductor to improve the converter dynamic. The proposed method has been simulated at the behavioral level using MATLAB and SIMULINK environment. Simulation results show that the proposed method have better dynamic response and low power consumption over the conventional sigma-delta controllers.**

***Index Terms*—Multi-bit, sigma-delta, PWM, SMPS, controller.**

I. Introduction

Low sensitivity to parameter variations, programmability and possibility of using more advanced control schemes are the main advantages of digital controllers in DC-DC converters concept. Digital realization allows the development of new control techniques that increase overall efficiency of the converter.

Digital regulation of output voltage of DC-DC converters has been an increasing demand for high dynamic performance power converters. Converter output voltage overshoot/undershoot and recovery time is often considered as the most important characteristics. Converter output voltage deviates under a load change, or an input voltage change. In order to improve the dynamic response of a dc–dc converter, the switching frequency and/or output filter can be regulated [1-3]. However, this method will result in either an increase in component cost or a decrease in efficiency. By improving the controller's dynamic response, the transient performance of a power converter can be improved without topology modification, thereby greatly reducing the component size and cost for high-performance converters.

In the past, typically only simple digital PI or PID controllers have been implemented. These control systems suffer from the limitations of slow compensator networks which degrade the dynamic performance of the converter [4]. With the emergence of powerful and low-cost digital signal processors (DSP's), digital control is becoming a potentially attractive alternative to the analog option. However, as compared to analog control, digital control suffers from a reduced control loop bandwidth due to the presence of time delays inherent to the digital control structure. Therefore, the improvement of digital control performance is a key issue that needs to be assessed and solved in order to make digital control a viable technological option.

The power consumption of the existing digital controllers is often comparable to that of the supplied low-power electronic loads which is resulting in a poor efficiency of the DC-DC converters. At higher switching frequencies the analog controllers take much less power, and consequently are more suitable solution, even though they do not posses most of the abovementioned features [5], [6].

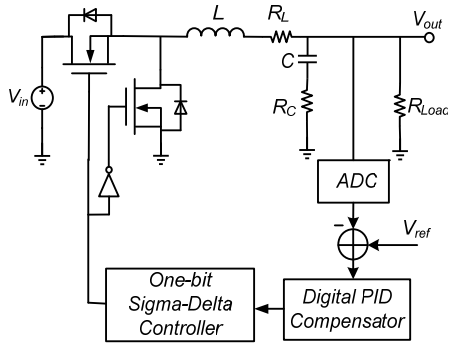

Fig. 1. Synchronous buck converter with conventional 1-bit sigma-delta controller.

One of the main limitations to maximum switching frequency at which digital controllers can be effectively used in low-power applications is the power consumption of digital pulse width modulator (DPWM). It is usually proportional to the product of the switching frequency and the DPWM resolution [1]. In addition, other functional blocks of digital controllers, analog-to-digital converters and compensators, usually take a significant amount of power, resulting in poor efficiency of low-power DC-DC converters. On the other hand, alternative digital architectures that do not require PWM signals, usually operate at non-constant switching frequencies creating wide-bandwidth noise, and as such, are not preferable in sensitive electronic devices. Because of that, constant-frequency DPWM controllers are still very interesting for low-power applications. High-resolution low-power DPWM controllers that operate at switching frequencies between 400 kHz and 2 MHz [4]. The higher frequency DPWM architecture cannot be used in portable devices either. It is designed for higher power DC-DC converters, where the power consumption of the controller is not so crucial. In addition at maximum switching frequency the resolution of the DPWM is low [1], [6], [7], [8].

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In most of the cases, this resolution is not sufficient.

In this paper, our main goal is to present a new architecture of low-power digital PWM controller for DC-DC converters that has very fast load-transient response. This architecture allows utilization of digital multi-bit sigma- delta controller. Fig. 1 shows a block diagram of the conventional digital sigma-delta controller regulating operation of a synchronous buck power stage. To achieve low power consumption low switching frequencies, a multi-bit second-order sigma–delta digital pulse-width modulator (second-order – DPWM) is used as shown in Fig. 2.

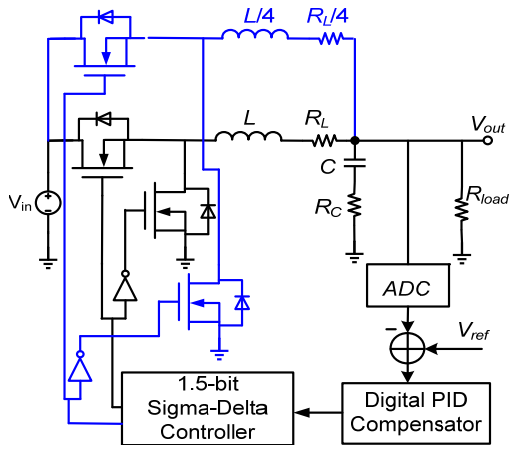

Fig. 2. Modified Synchronous buck converter with 1.5-bit second-order sigma-delta controller.

II. Digital Multi-Bit Sigma-Delta Controller

A. Sigma-Delta Modulator

Most of the existing DPWM architectures are not well-suited for operation at low switching frequencies. They either rely on power consuming counters operating at frequencies several-orders of magnitude higher than the converter switching frequency .The resolution of DPWM, i.e., its time quantization steps, is constrained by the method that used for it. To minimize requirements on the resolution of DPWM, dithering and sigma–delta architectures that increase effective resolution of the DPWM through averaging process are developed [1]. DPWM base on sigma-delta modulator consists of a low-resolution low-power DPWM capable of operating at high switching frequencies and a sigma-delta modulator, which improves effective resolution of the core DPWM. The sigma-delta operation is based on the well known noise-shaping concept widely used in analog-to-digital and digital-to-analog converters [8]-[12]. Over several switching cycles, the modulator varies the low-resolution input of the core DPWM, between few possible values to achieve a high-resolution average duty ratio value. When connected to a switching converter as shown in Fig. 2, no additional hardware is needed for averaging. It is naturally performed with the filtering components of the converter.

Several design aspects of multi-bit sigma-delta converters must be considered. These models allow the designer to determine the required specifications for the different building blocks and form the basis of a systematic design procedure [4].

Multi-bit sigma-delta architecture eliminates the need for power dissipative high-frequency high-resolution DPWM and consequently allows efficient operation at high switching frequencies.

The proposed sigma-delta controller for DPWM shown in Fig.2 is based on the well-known sigma-delta modulation concept. As shown in Fig. 3, it consists of a low-resolution DPWM (Quantizer), a delay block, and two adders. second order sigma delta controller was selected which is inherently stable [8]. The coefficients (a_1, a_2, $a_3$and a_4) are calculated by using toolbox of Schreier [8]. The output signal of compensator, a multibit digital signal, enters to sigma-delta modulator. A two signal is needed to active and inactive the MOSFET switches and also its complementary MOSFET switch for synchronous mode. Therefore the output signal of sigma-delta modulator should be a 1.5-bit signal. The quantizer, shown in Fig. 3, transfers two most significant bit of its input signal and truncates its other bites. This operation adds a truncation error or a quantization noise to the signal. The quantization noise has correlation with input signal and causes linearity error at the output of the controller. According to Fig. 3, before truncation of multibit input signal of sigma-delta modulator, X, to a single-bit signal, Y, the sigma-delta modulator preprocesses its multibit input signal in a closed loop system like what is shown in Fig. 3. During this preprocessing, which is arise in the sigma-delta feedback loop, the quantization noise is shaped and transmitted to high frequency part of sampled frequency-band. Also the correlation of input signal and the quantization noise signal is considerably eliminated by sigma-delta loop [8]. The linear model of quantizer of Fig .3 is an additive quantization noise. By this assumption, respectively the signal transfer function and noise transfer function of sigma-delta loop of Fig. 3 in Z-domain are:

$$STF = \frac{a_3 a_4}{z^2 + (a_2 - 2) z - a_2 + a_1 a_4} = \frac{0.01}{z^2 - 1.75 z + 0.85} \quad (1)$$

$$NTF = \frac{(z-1)^2}{z^2 + (a_2 - 2) z - a_2 + a_1 a_4} = \frac{(z-1)^2}{z^2 - 1.75 z + 0.85} \quad (2)$$

It is evident from (1) and (2) that the STF is a low pass filter while NTF is a high pass filter. On the other hand, for a reasonable value of oversampling ratio (OSR), the low-frequency input signal, X, appear at the output of sigma-delta with no frequency shaping. In contrast the broad-band quantization noise is completely frequency shaped. The quantization noise is rejected in the low frequencies and just its high frequency components appear at the output of sigma-delta.

For the case shown in Fig.2, the low-resolution DPWM is a 1.5-bit Quantizer that changes duty ratio of the pulse-width modulated signal between three possible values: -1, 0, 1. The duty ratio is varied over several switching periods to result in an average value that has high effective resolution. The high resolution is necessary for the tight output voltage regulation and for the elimination of undesirable quantization effects. The value of the duty ratio is set by the high-resolution digital control command and the averaging process is performed by the switching converter itself. The effective averaging is possible as long as the corner frequency of the converter

satisfies the following condition:

$$f_C = \frac{1}{2\pi\sqrt{LC}} < f_{sw} = \frac{1}{T_{sw}} \quad (3)$$

where T_{sw} is the averaging period. The fast convergence toward the high-resolution value, i.e. short averaging period, is provided with the internal loop of the sigma-delta DPWM, and effectively increases the resolution of the internal DPWM.

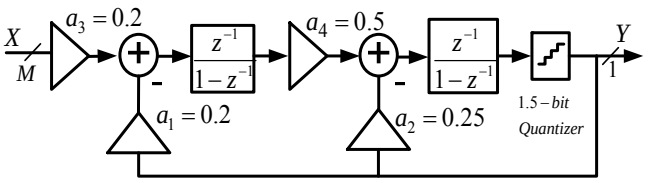

Fig. 3. Block diagram of a multi-bit sigma-delta DPWM (Σ-Δ DPWM).

To find the effective resolution of the sigma-delta DPWM general analysis of the sigma-delta concept can be used, which is based on the signal-to-noise ratio (SNR) comparison [4]. The analysis shows that sigma-delta modulation improves the resolution of the internal DPWM by 1.5 bits with every switching period added to the averaging sequence. It can be shown that, in the system of Fig.2, the effective resolution of 4.5 bits can achieved by averaging the output of the 1.5-bit DPWM over 2.5 switching periods.

So, in comparison with conventional PWM, digitally controlled converters need high frequency PWM while this can be resulted with low frequency multi-bit sigma-delta.

B. PID controller

In this paper for comparison achieved results from proposed technique, the conventional sigma-delta controller is considered too. In both cases, for compensation purpose, a conventional PID with the following equation is used:

$$H(z) = \frac{z^2 - 1.95z + 0.95}{z(z-1)} \quad (4)$$

The parameters of this compensator are achieved from stability view as explained in [6].

III. Simulation Results

The synchronous DC-DC buck converter of Fig. 2 with its sigma-delta controller was simulated in MATLAB and SMULINK environment. The parameter of circuit was chosen as: L = 4μH, C = 180 μF, R_C = 0.04 Ω, R_L = 0.01 Ω. The controller parameters are: f_S = 2 MHz. The performance of converter with 1-bit sigma-delta modulator and proposed technique are shown in Fig. 4. All specifications of the circuit of converter were fixed in both simulations. Sampling frequency of 1-bit sigma-delta was 4 MHz while for 1.5-bit sigma-delta ADC is 2MHz. As illustrated in Figs. 4 and 5 the efficiency of proposed technique is significantly better than PWM controller.

Multi-bit controller of converter was simulated and its influence on efficiency per load current curve of converter was survived. As illustrated in Fig. 6. In light load, the efficiency of 1-bit sigma-delta is degraded while the efficiency of Multi-bit controller is maintained.

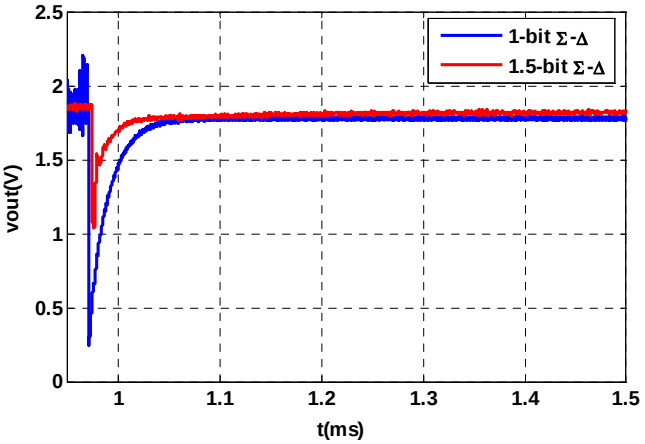

Fig. 4. Efficiency comparison of 1-bit sigma-delta modulator and proposed technique in load variation.

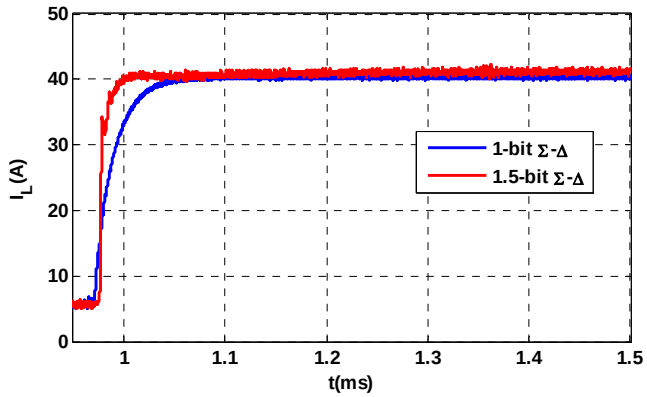

Fig. 5. Inductor current comparision of 1-bit sigma-delta modulator and proposed technique in load variation.

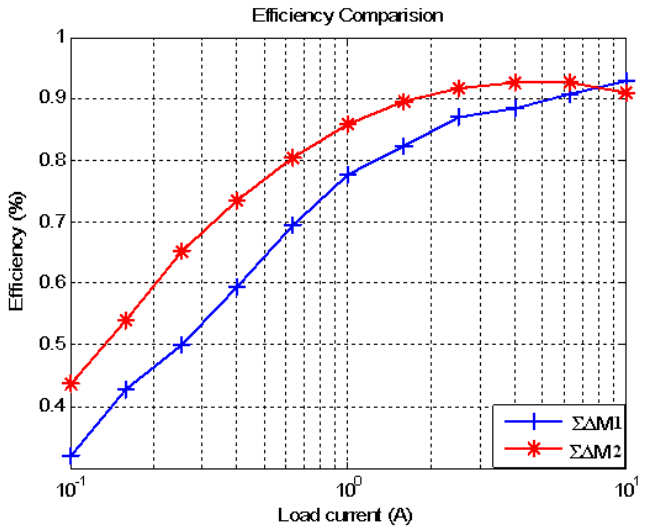

Fig. 6. Efficiency comparison of 1-bit sigma-delta modulator and proposed technique.

IV. Conclusion

A digital Multi-bit sigma-delta controller for synchronous DC-DC buck converter was described in this paper. The simulation results of a synchronous buck DC-DC convertor with 1.3 V output, 8.5V input, were presented. Simulation results show that Multi-Bit controller has an excellent efficiency over wide range of load variations. Also

simulation results predict that the proposed technique significantly improves the efficiency of converter compared to conventional PWM controller and conventional sigma-delta controllers. The method has about a number of advantages: the design is small and the overall power consumption will be very low. Due to the oversampling in sigma-delta modulator, design consideration such as mismatch requirement can be less stringent. In addition, PID control is made possible in the analog or in the digital domain making the design flexible and furthermore, The PWM power-switching scheme makes the design suitable for the portable low-power applications.

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