Clock Gating Implementation on Direct Memory Access

Shabagran Gandi, Zulfiqar Ali, and Suphachai Sutanthavibul

***Abstract*—This paper discusses about the implementation of a low power design technique, clock gating, on Direct Memory Access (DMA) at Register Transfer Level (RTL). Modification has been done to the existing clock gating circuitry by adding and utilizing the reset signal of a register as an additional enable pin. The modification approach and the method to identify appropriate clock gating candidates have been discussed. The power consumptions and few other factors including speed and area were estimated. The results were compared with two different methods of clock gating implementations, fine-grain clock gating and global clock gating. A total of 38% of dynamic power reduction has been achieved when both, global clock gating and fine-grain clock gating were implemented simultaneously.**

***Index Terms*—Clock gating, dynamic power,leakage power, and low power VLSI design.**

I. Introduction

Today, as the size of transistor shrinks, the number of transistors in a System on Chip (SoC) has attained billions [1]. This has been the main driving factor for the applications enhancement in SoC design [1], [2], [4]. However, there are few challenges that need to be faced by integrated circuit (IC) designers. As they attempt to mount additional features in the SoC design, performance, area, and power need to be maintained fairly [1], [2], [7]. Among these factors, uphold the power consumption of a SoC design has been a great challenge over the years [2], [5]. One approach to tackle this power issue is by enhancing the packaging technology of an IC. Conversely, upgrading the packaging technology will lead to the increase of overall packaging cost [7].

TABLE I: Summary of Power Savings At Each Design Level

Design Levels	Low Power Technique	Power Savings (%)
System Level	Dynamic Voltage Scaling	50-90
RTL	Clock gating, operand isolation	30-50
Gate Level	Technology mapping, gate resizing	20-30
Circuit Level	Pass gate logic, transistor sizing	10-20

Alternatively, most designers practice appropriate low power design techniques at different design levels to resolve the power issue. Table I below summarizes the low power design techniques at each design levels with their respective percentages of power savings [2], [4].

This paper will be discussing on clock gating technique and its implementation on DMA. Section II of this paper discusses about the power dissipations within a CMOS circuit. The overview of clock gating technique is reviewed in Section III. The implementation of clock gating technique on DMA and the results are elaborated in Section IV. Section V is the conclusion and followed by Section VI, the authors' future work.

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II. Power Dissipation in CMOS Circuits

Power dissipation in CMOS circuits can be classified into two different power categories, dynamic power (P_{DYN}) and leakage power (P_{LEAK}) [7]. P_{DYN} is the summation of switching power (P_{SWI}) and short-circuit power (P_{SC}) [6]. Mathematically, total power consumption (P_{TOT}) of an IC can be represented as [1], [3], [4]:

$$P_{TOT} = (P_{DYN}) + (P_{LEAK}) \quad (1)$$

$$P_{TOT} = (P_{SWI} + P_{SC}) + (P_{LEAK}) \quad (2)$$

A. Switching Power (P_{SWI})

P_{SWI} is dissipated due to the charging and discharging activity of the output capacitance in a CMOS circuit [8]. The equation to calculate P_{SWI} is

$$P_{SWI} = (C) \times (V_{DD}^2) \times (f) \times (\alpha) \quad (3)$$

where C is the total capacitance, V_{DD} is the supply voltage, f is the operating frequency, and αis the switching activity [3], [4].

B. Short Circuit Power (P_{SC})

P_{SC} is dissipated when both, PMOS and NMOS transistors of a CMOS circuit are turned on simultaneously for a short interval of time [1], [6]. P_{SC} is given by

$$P_{SC} = (I_{SC}) \times (V_{DD}) \times (f) \quad (4)$$

C. Leakage Power (P_{LEAK})

P_{LEAK} is dissipated at gate in a CMOS circuit when the circuit is not switching [3]. P_{LEAK} is givenby

$$P_{LEAK} = (I_{LEAK}) \times (V_{DD}). \quad (5)$$

$$P_{LEAK} = (I_{SUB} + I_{GOX} + I_{GIDL} + I_{DREV}) \times (V_{DD}). \quad (6)$$

where I_{SUB} is the sub-threshold leakage current, I_{GOX} is the gate oxide leakage current, I_{GIDL} isthe gate induced drain leakage current, I_{DREV} is the diode-reverse bias current leakage current and V_{DD} is the supply voltage [1], [6], [8].

III. Clock Gating

The clock network in a chip dominates the major portion of

the dynamic power dissipation [8]. In reality, the clock signal toggles every cycle even though the utilization of the clock signal is not complete [6]. Clock gating, a low power design technique, has the ability to limit the toggling frequency of a clock, so that it will only toggle when it is necessary [6], [8]. Fig. 1 below shows the timing diagram of the input clock (CLK) and gated clock (gCLK). After the clock is gated, all the redundant clock cycles have been removed and this will lead to the minimization of the clock's toggling frequency.

P_{DYN} will be reduced when all the redundant clock cycles are removed by implementing clock gating technique [9], [10], [12]. By referring to "(2)," there are two components of P_{DYN}, P_{SWI} and P_{SC}. Specifically, clock gating implementation will reduce the P_{SWI}. Refer to "(3)," it can be seen that the computation of P_{SWI} is based on four factors, the capacitance, voltage, frequency and switching activity. Clock gating technique reduces the switching activity (α) factor of P_{SWI} [11]. Fig. 2 below is an example that shows the relation between P_{SWI} and switching activity.It can be seen that as switching activity increases, P_{SWI} increasesas well. Hence, via clock gating technique, switching activity factor will be minimized which will reduce the P_{SWI}.

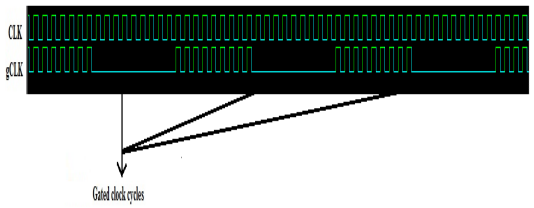

Fig. 1. Timing diagrams for clock signal and gated clock signal

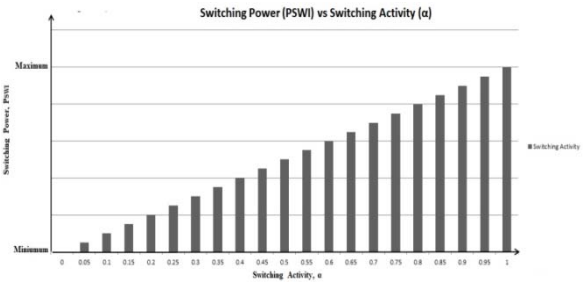

Fig. 2. Graph of switching power versus switching activity

A. Fine Grain Clock Gating (FGCG)

FGCG technique is implemented within a functional unit block. The implementation approach for FGCG can either be automatic insertion (static clock-gating) or manual modification of RTL [10]. Static clock-gating is a standarddesign of clock gating circuitry which is inserted to all appropriate clock gating candidates using Electronic Design Automation (EDA) tools. Most of the current EDA tools come with this feature [8], [10]. The most common clock gating candidate is the feedback multiplexer [10]. Fig. 3 below illustrates the architecture of FGCG implementation to a feedback multiplexer.

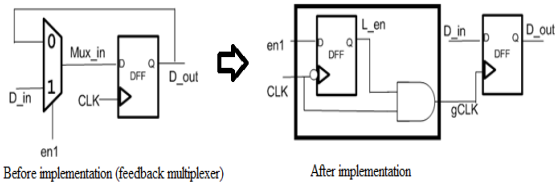

Fig. 3. FGCG implementation

B. Global Clock Gating (GCG)

GCG technique applies the similar concept of FGCG but it is done at very top level of a functional unit block. GCG can only be done by manual RTL modification. GCG needs designers' attention about the functional behavior of the block before attempting to gate the clock [10]. GCG is much more significant since it has the ability to shut off the clock signal of a functional unit block or the entire unit when it is in idle condition. This will lead to the maximization of the battery life of a system [7]. Fig. 4 below shows the concept of GCG.

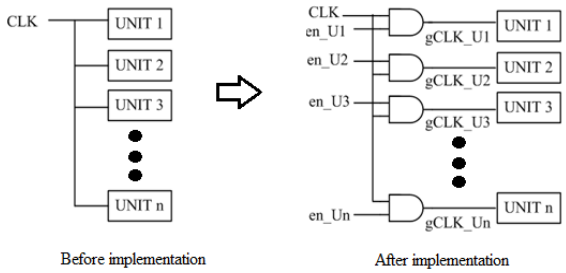

Fig. 4. GCG implementation

IV. Discussion

Both, FGCG and GCG have been implemented on DMA by manual modification at RTL level. The existing FGCG architecture was modified for the implementation on DMA. The modification strategy that was done to the standard FGCG are shown on Fig. 5 below.

The modification is actually the utilization of the reset signal as an additional enable signal to trigger the clock.For the reset signal to be utilized as an additional enable signal, the computation that based on the reset signal should not be clock dependent. Besides feedback multiplexer, other candidates that have been considered for this type of clock gating were standalone registers with reset signal. Fig. 6 below illustrates the proposed implementation approach on the stand alone registers.

Although there were 70 registers with corresponding architecture, only 52 registers were selected as appropriate candidates for this type of implementation. Screenings were done based on their number of bits so that, the number of AND gates to be used can be reduced. Unconstrained AND gates for clock gating technique will affect cost and timing.

Fig. 7 below shows the percentage reduction of P_{DYN} versus the number of bits. As can be seen, the proposed implementation approach increases the P_{DYN} for registers with one bit to four bits. In other words, implementing this type of architecture to registers with four bits and below is actually an overhead.

From the same Fig.7, the reduction percentage seems to be increasing for registers with eight bits onwards. Almost 20% of reduction can be achieved for registers with 12, 16, 24, 28, and 32 bits. Hence, it can be concluded that, it is more appropriate to implement the proposed modification on registers with more than eight bits. This theory was used for the modified FGCG candidate selection.

Fig. 8 below illustrates the timing diagrams for FGCG and GCG. By comparing with main clock (CLK), some redundant clock cycles were eliminated after GCG

implemented (gCLK_GG). When GCG and FGCG (gCLK_FG) implemented mutually, significant number of clock cycles have been reduced. This shows the influence of mutual implementation of GCG and FGCG.

Table II shows the complete power saving percentages that obtained from both FGCG and the combination of GCG and FGCG implementation on DMA. These percentages are with respect to the original design. P_{DYN} decreased by 38% when GCG and FGCG were implemented simultaneously. Besides, the overall power consumption of DMA has reduced by 6.5%.

With these types of implementations, the clock gating efficiency has increased 27.6%. The power reductions are reasonable with this approach, but it has to tolerate the timing, which is affected by 33.3 %.

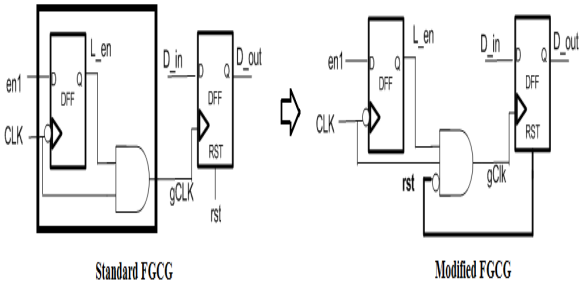

Fig. 5. Modified FGCG implementation

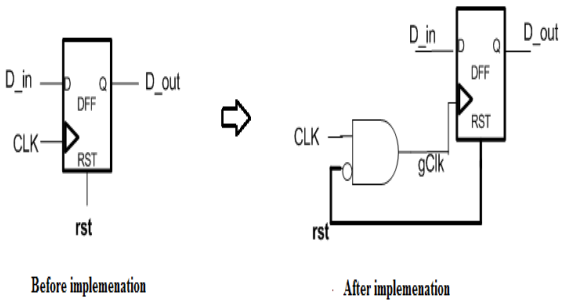

Fig. 6. Modified FGCG implementation on standalone registers

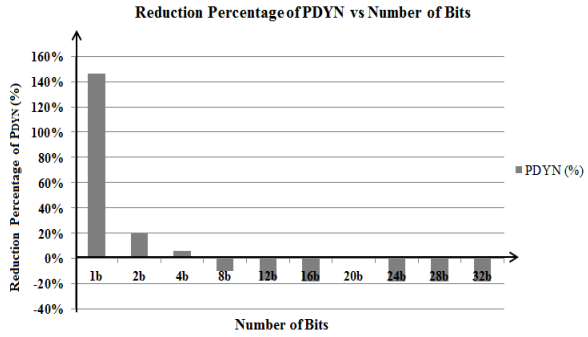

Fig. 7. Graph of reduction percentage of P_{DYN} versus number of bits

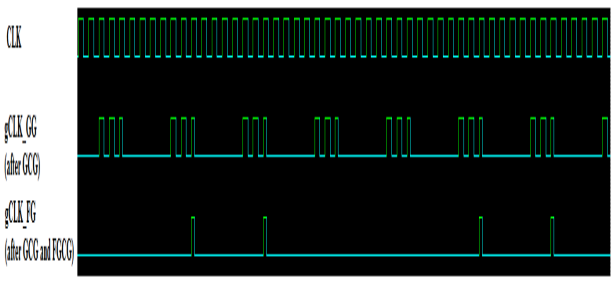

Fig. 8. Timing diagrams of clock signals after FGCG and GCG implementation

TABLE II: POWER RESULTS

Types of power	FGCG	GCG + FGCG
P_{SWI}	+14.8 %	- 8.3 %
P_{SC}	- 10.5 %	- 51.1 %
P_{DYN}	- 2.8 %	- 38.0 %
P_{LEAK}	- 3.1 %	- 6.5 %
P_{TOT}	- 3.1 %	- 6.5 %

TABLE III: OTHER FACTORS RESULTS

Other factors	FGCG	GCG + FGCG
Number of cells	+ 7.10 %	+ 6.00 %
Area	+ 0.95 %	- 0.05 %
Timing	+ 16.67 %	+ 33.33 %
Number of clock gates	+ 63.60 %	+ 72.70 %
Efficiency	+ 7.00 %	+ 27.6 %

V. CONCLUSION

In brief, optimal enable signals for both FGCG and GCG have been identified and utilized for implementation on DMA. Significant amount of power was reduced with the combination of GCG and FGCG techniques. FGCG technique reduces P_{DYN} by 2.8%, but drastic increase in reduction percentage was observed when both GCG and FGCG were implemented mutually. The P_{DYN} has been reduced by 38% with the combination of GCG and FGCG, which is about 13 times more than what was achieved with only FGCG implementation. The power consumption was reduced significantly with the proposed approach, but the speed was slightly affected. Timing has to be sacrificed if the power reduction is the sole concern.

VI. FUTURE WORK

Currently, the authors are attempting to identify more opportunities to enhance the GCG implementation on DMA as it shows great reduction of P_{DYN}.

There are seven channels that available in DMA and only one channel will be serviced at a time. Hence, as further improvement, authors are also attempting to gate the clock of the unused channels in order to enhance the power reduction.

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