An FPGA-Based Controller for High Speed Train System

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***Abstract*—The progress of programmable logic devices such as FPGA makes it realize the digital control system without microprocessor recently. A very complex control algorithm can be implemented into FPGA and the calculation time can be dramatically reduced based on parallel processing hardware circuit. In this paper, a design conceptual of original FPGA-based controller for high speed train system is proposed. The Cyclone-II EP2C35F672C6 with EPCS16 16-Mbit serial configuration device is based on SRAM technology and nine embedded array blocks (EABs) are implemented. Based on the simulation result and hardware implementation, the FPGA speed controller has very good performance in controlling high speed train system.**

***Index Terms*—Controller, field programmable gate array (FPGA), hardware, high speed train.**

I. Introduction

All high-speed railway systems have brought up many new and challenging technical issues as well as commercial issues such as transport capacity, comfort and safety. The railway systems can work with high security and high efficiency are mainly depended on the core of the train control systems. Much effort has been made to study, understand and analyze on automatic train control systems over the years [1]-[3]. It is a typical complex dynamic system with large time delays, a high nonlinearity and multi objectives, which is under time-varying and uncertain conditions on such parameters as traction power supplies, different type of signals, speed restrictions, braking and so on. In real operation, different situations imply different control demands for different purposes, while the main objectives are always on-time scheduling, high speed motion, full load and most important safe operation of the train. A high-speed train motion and operation is a complicated, complex system and process, involving locomotive dynamics, communications and signaling, rail track, etc. for which simulation systems provide a practical platform for design, testing and analysis [4], [5]. Due to the high complexity and diversity of automatic train control systems, good computer based simulation tools for evaluation of the effectiveness of new protocols and the feasibility of new applications are greatly importance.

An FPGA is a device that contains a matrix of reconfigurable gate array logic circuitry. When an FPGA is configured, the internal circuitry is connected in a way that creates a hardware implementation of the software application. FPGA technology provides the reliability of dedicated hardware circuitry, true parallel execution, and lightning-fast closed-loop control performance. As a result, the performance of one part of the application is not affected when additional processing is added. Also, multiple control loops can run on a single FPGA device at different rates. FPGA-based control systems can enforce critical interlock logic and can be designed to prevent I/O forcing by an operator. However, unlike hard-wired printed circuit board (PCB) design, which have fixed hardware resources, FPGA-based systems can literally rewire their internal circuitry to allow reconfiguration after the control system is deployed to the field. FPGA devices deliver the performance and reliability of dedicated hardware circuitry [6].

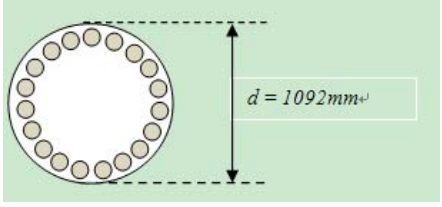
The modeling, simulation and prototype of high-speed railway systems and particularly its automatic control system are analyzed and demonstrated on FPGA.

II. Hardware Implementation

Hardware implementation for this controller is divided into three sections which cover the velocity, distance and auto-throttle.

A. Velocity Meter

Velocity is a rate of displacement change. The scalar absolute magnitude of velocity is a speed which is usually used to measure in kilometer per hour (kmh−1). In hardware implementation, 14 bits parallel adder is used with two inputs; A and B to calculate the velocity. A value for input B is preset to $0x01101_2$. The outputs of parallel adder are connected to a 14 bits register (R1) with a clock name PULSE. The outputs from this register are passing back to the parallel adder as input A. PULSE is a signal to trigger the inputs of R1. Once the PULSE in rising edge, the outputs of R1 will pass to the parallel adder and adds up with input B. Function generator is used to generate PULSE in different hertz to represent the number of cycle per second of the wheel movement. Nineteen signals are considered for each cycle of a wheel which means that for every 19Hz the train movement with the velocity of 12.35 kmh−1. The velocity is obtained by (1):



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Velocity (km/h) = velocity (m/s) × 60 × 60 / 1000

Velocity (m/s) = distance (m) / time (s) (1)

(Distance = πd, where, d = 1092mm)

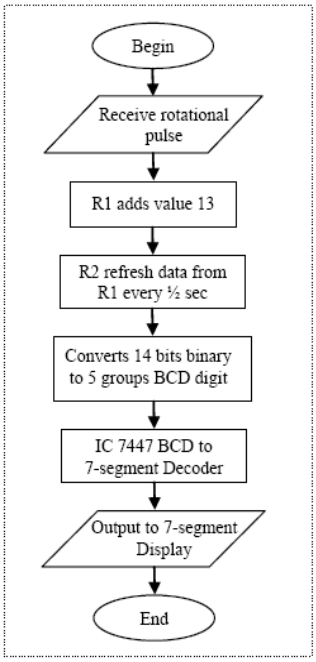


Fig. 1. Flowchart of velocity method

Fig. 1 shows a flowchart of the velocity procedure. This will be used for the base unit calculation of velocity. By dividing this velocity to 19, we will get a value of 0.65 which is the velocity for each signal passing. Since the memory is updated for every half second, this value is doubled becomes 1.3 kmh−1. The decimal point is ignored and it becomes 13. So, $0x01101_2$ (13_{10}) becomes the constant for each signal passing in half second. The instantaneous velocity calculated by parallel adder (R1 outputs) will pass to another register,R2. R2 will then store and updating the value of velocity for every half second to be displayed in 7-segment for the next stage. The R2 is controlled to run and updated every half second with a counter mod-5000 by clock division of 10kHz. For every 4999 cycle in the mod-5000 counter, the memory inside the R2 will be updated. After the memory updating process in R2, R1 will be reset to 0 by the counter mod-5000. Hence, the velocity for the next half second will start to calculate through parallel adders. This process recycles to get the current velocity to be displayed. The ouputs of R2 will pass a 16 bits binary to BCD converter. Each 4 bits of BCD number will be connected to 7447 chip to generate the outputs for 7-segment.

B. Distance Meter

The calculation of distance travel by the train is based on the number of pulse that triggered by the wheel. Inside the distance meter block, there is a mod-19 counter to count the number of pulse that triggered by train's wheel. The distance meter is connected to the pulse input which having a same source with the velocity meter. The outputs of the distance meter are displayed on 7-segment. Distance travelled = (wheel's perimeter) x (number of wheel's cycle) as shown in (2).

19 signal pulse = 1 cycle of wheel ;

1 km / 3.432m = 291.37 cycles (2)

Hence, 19 pulses x 291 = 1 km

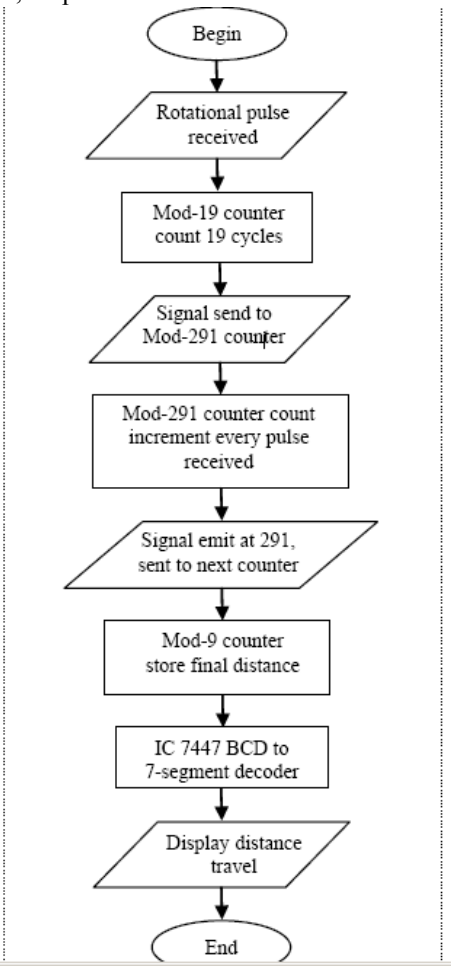


Fig. 2. Flowchart of distance meter

Fig. 2 shows the flowchart of how the distance is calculated for this system. Mod-19 counter will count the number of pulses that being inserted until pulses-19th and then triggering a pulse to next counter, which is mod-291 counter. It will reset the counter again when pulse-20th. The second counter will count until 291 cycles. When the counting reach a pulses of 291, this means that a train has travel for a distance of 1km. Then, a pulse will trigger the mod-9 counter to display. Each modulo can only count from 0 until 9 meaning that a maximum distance traveled can be displayed upto 999km. The distance will be cleared and recounted. The maximum distance travel can be increased by adding additional mod-9 counter into the system design.

C. Auto-Throttle Control System

Most designed of auto-throttle system is basically same as the one used on the aircraft. It allows a pilot to control the power setting of an aircraft's engines by specifying a desired flight characteristic rather than manually controlling fuel flow. This system can help to conserve energy reduce to the machine operator workload. Meanwhile, the similar system can also be applied on a train. The train system usually is controlled by the operating centre but this actually is not very secure. In order to reduce the human factor error, the auto-system is needed to operate the train. The system design

practically has 3 operating modes as shown in Fig. 3; Normal Break (NB), Increase Throttle (IT) and Hold Throttle (HT). First, the instantaneous velocity values that comes out from the velocity meter will be fed to the comparator. Then, a velocity limit is assigned as our safe velocity limit. The comparator will then compare both velocity values.

The NB mode is designed to decrease the train speed. The first counter will counting for 5 seconds. After that, it sends a signal to the throttle control register to increase the resistance, which simultaneously reduce the power supply of the motor and finally reduce the train velocity. The throttle register will reduce one resistor at a time. After one resistor being increased, another counter will counting for 7 seconds. If the velocity is still higher or lower than the set up of velocity limit then the counter will send a signal to the previous counter to count 5 pulses and increase the resistor value again to reduce the velocity. These steps will take place alternately until the velocity of the train reach the assigned velocity.

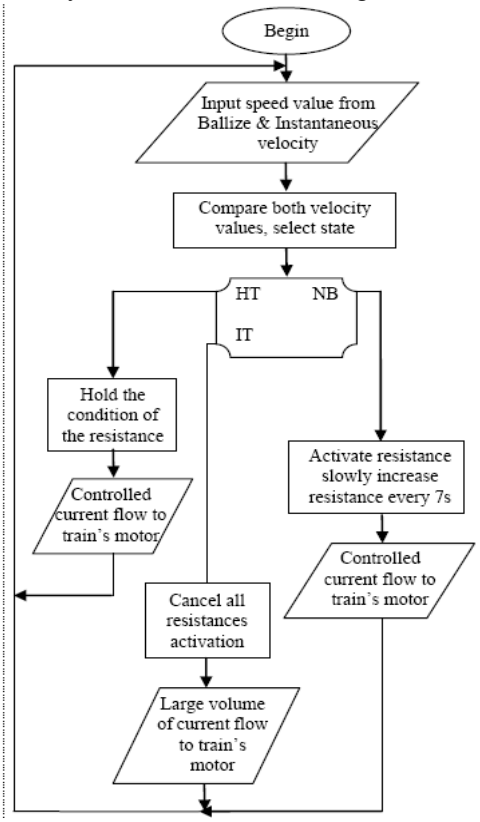


Fig. 3. Flowchart of auto-throtte control system

Meanwhile, in the IT mode, only the lowest value of resistor is being activated. Other resistors will be turned off at the same time. So, when a resistance is very small, the power supply will increase drastically and at the same time the motor will be accelerated.

Lastly, the HT mode activation is progressed. This mode is used by the train to maintain the speed of it. Initially, a velocity value is assigned to the comparator. The velocity meter is connected to the comparator. If the velocity of the train is lower than the assigned velocity, the HT mode will be deactivated. It will decreases the values of resistor, increase the power supply and the motor power in order to reach the assigned velocity.

The design system consists of 2 blocks of 4 bits comparator, mod-5 and mod-7 counters, states define logic circuit (NB, IT, and HT) and shift registers. It will firstly comparing the instantaneous velocity with the limit velocity. When

- instantaneous velocity larger then (>) limit velocity, 'NB State' will be activated.
- instantaneous velocity smaller then (<) limit velocity, 'IT State' will be activated.
- instantaneous velocity equal to (=) limit velocity, 'HT State' will be activated.

III. Discussion

This velocity meter is able to measure the velocity maximum up to 1638.3 kmh-1. This is because of the system design use 14 bits register. When the register adds up to 11111111111111_2 ,then the value becomes 16383. In order to obtain an accurate velocity, the clock pulse use to refresh R2 in the design needs to be as sharp as possible. The sharper the signal, it will less disturb the addition operation in the adder. Besides the influence to the addition operation, this 2 Hz signal also needs to clear the R1. Hence, there are 2 signals emitted from the mod-5000 counter. The first signal will refresh the R2 while the second one will reset R1. But these 2 processes need to be done in almost the same time. Hence, 10 kHz clock is used to trigger the refresh 2 Hz signal for the R2. A maximum of 14 bits data are able to be calculated by the adder. When these 14 bits of data converted to the BCD, there will be 4 groups of BCD values. These 4 groups of BCD will consist of 3 digit numbers and 1 decimal value to represent the instantaneous velocity.

The conversion of 14 bits binary values into BCD is using 74185 chip. The converting module is based on the sample application from the datasheet. But the module is able to convert 16 bits binary to 5 groups of BCD. Since the output of the BCD to 7-segment display needed in the design is active-LOW, hence 7448 chip is chosen to decode the BCD digit in the system to reduce the number of gates. The probe of the signal generator use to generate the signal pulse in the system needs to be grounded. This is because the generated signal will have many fluctuations and this may interupt the entire system. There are only positive square wave outputs are required to drive the system. The negative cycle of signal will be delivered to the system. The decimal point on the 7-segment display cannot be fed directly by supply voltage, VCC. When the decimal point pin directly fed by the VCC, the VCC will then shut down all the segments of display and show all active-LOW. The auto-throttle system is mainly controlled by the on/off switch. We can activate the system according to our need and desire. The display velocity will have a small difference compared to the actual value of velocity due to time delay on the addition operation and unstable of frequency which was generated from the function generator.

IV. Results

The logic resources required for the components of the system design running on Cyclone-II EP2C35F672C6 with EPCS16 16-Mbit serial configuration device are shown in Table I. The system operates at the frequency of 50MHz.

TABLE I: LOGIC RESOURCES FOR THE SYSTEM DESIGN

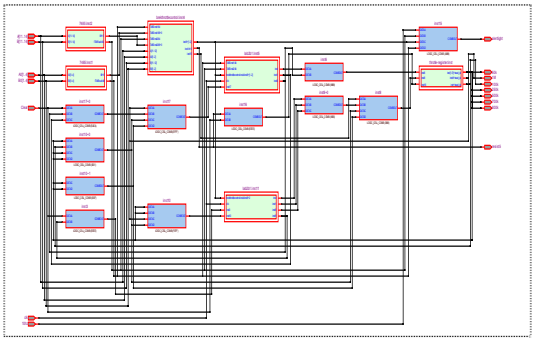
Resources Type	Resources Type
Total logic elements	44
Total combinational functions	38
Registers	14
I/O Pins	28
Maximum fan-out	8
Total fan-out	173
Average fan-out	2.4

Appendices A and B show the structure of the auto-throtte technolgy map viewer and RTL viewer, respectively.

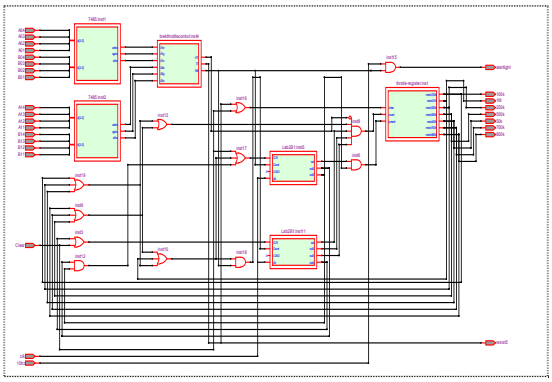
V. CONCLUSION

The design conceptual of original FPGA-based hardware controller system is proposed. The system was successfully compiled and simulated. The hardware implementation demonstrates complete, correct functionality and met all the initial system requirements. This may be widely applied to many vehicle applications. Demonstration of experimental result with single rate control of 50MHz system was carried out, and verified proper operation of the proposed FPGA control board.

APPENDICES



A: Technology map viewer of auto-throttle structure



B: RTL viewer of auto-throttle structure

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