A New Soft Switched Full Bridge Converter With Voltage-Doubler-Type Rectifier for High Voltage Applications

V. Delbin Jelaja and M. Rajaram

***Abstract*—A new soft switched full bridge converter with voltage doubler type rectifier is proposed to reduce the circulating loss in primary and the voltage stress in secondary. The conventional converter is having the drawbacks such as circulating loss in the primary, voltage spike across the rectifier diode. Also the conventional system is using large output inductor in the secondary side, because of this core loss occurs. In this paper we introduce a new technique to overcome the above said drawbacks. Without an auxiliary circuit, zero – voltage switching (for leading - leg switches) and zero – current switching (for lagging – leg switches) are achieved in the entire operating range, which reduces the circulating loss in the primary side. To implement the converter without an additional inductor, the leakage inductance of the transformer is utilized as the resonant inductor. The resonance between the leakage inductance of the transformer and the rectifier capacitor can reduce the current stresses of the rectifier diodes and the conduction losses. The clamp diode is used to clamp the voltage spike across the rectifier diode which releases the voltage stress of the rectifier diode. Due to its many advantages this converter is attractive for high voltage and high power applications. The analysis and design considerations of the proposed converter are presented. The simulation results confirm efficiency above 98% which is 3% to 5% more than the conventional converters.**

***Index Terms*—Phase shift full bridge (PSFB) converter, zero– voltage and zero – current switching (ZVZCS), voltage - doubler – type rectifier**

I. Introduction

The zero - voltage and zero – current switching converters are very attractive for high voltage and high power applications. The phase shifted ZVS PWM converter is often used in many applications because its topology permits all switching devices to operate under zero–voltage switching by using circuit parasitics such as power transformer leakage inductance and the rectifier capacitors. However, because of Phase Shifted PWM Control, the converter has a disadvantage that circulating current flows through the power transformer and switching devices during freewheeling intervals. The circulating current is the sum of reflected output current and transformer primary magnetizing current. Due to the circulating current, root mean square (RMS) current stresses of the transformer and switching devices are still high compared with those of the conventional hard- switching PWM FB converter. The zero-voltage and zero–current switching (ZVZCS) technique is proposed based on PSFB converter to reduce the circulating loss. The key point of this technique is to use the leakage inductance of the transformer as resonant inductor, with the help of that we can achieve Zero–voltage, zero–current

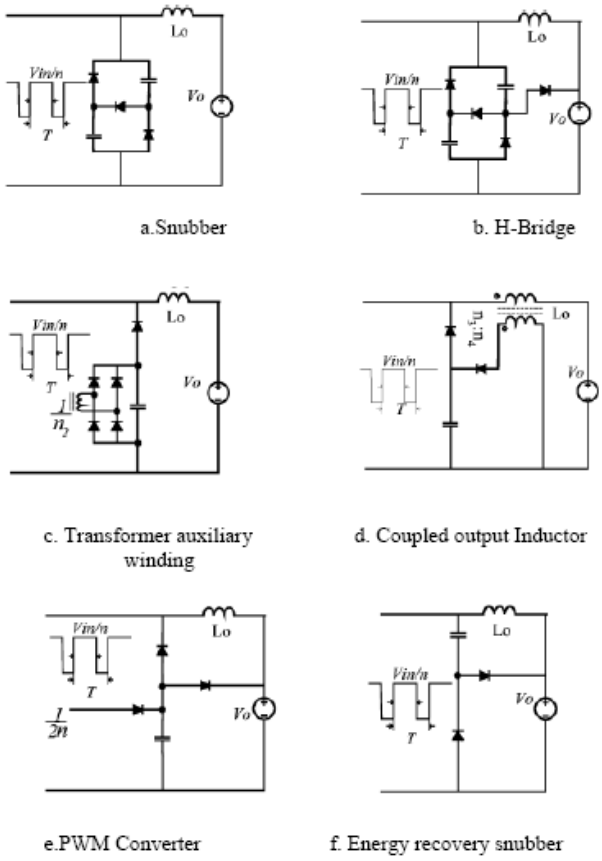

Fig. 1. Previous Secondary sides current reset circuits.

Switching in the entire operating range. The conduction loss is high [1] for the diode in series with primary switch due to the large primary current, though the circulating loss can be eliminated. Inserting an auxiliary inductor with three coupling windings in primary side of the transformer [2], primary current is reset by input voltage source through the auxiliary coupling windings in the transformer, but the conduction loss in auxiliary circuits is large because of high input current, and the voltage ringings across the rectifier diodes are still high. By an active switch in secondary side [3], [4], the primary current in transformer can be reduced. But the control is complex because the auxiliary switch should be driven corresponding to the driving logic of the primary switches. In [5] the primary current is reset by utilizing dc blocking capacitor and adding a saturable inductor in the primary. In spite of the simple additional circuit, this converter is not suitable for high power

Manuscript received February 27, 2012; revised March 30, 2012.
V. D. Jelaja is with Anna University, Chennai,India.
M. Rajaram is with Anna University of Technology, Tirunelveli, Tamil Nadu, India.

applications due to the core loss of the saturable inductor. Fig 1 represents the previous secondary side current reset circuits. Fig 1(a) shows the snubber circuit. Here the peak voltage across the rectifier can reach twice of the steady state value. Fig 1(b) shows the H-bridge snubber. Here the lossy components are more, voltage stress across the rectifier reaches twice of the steady state value and large circulating current flows through the primary which reduces the overall system efficiency. Fig1(c) represents the transformer auxiliary winding, which increases the complexity of the transformer and it requires additional RC/RCD snubber. Fig 1(d) shows the coupled output inductor, here the voltage across the rectifier cannot be reduced properly and the switching noise can also be more.
Fig 1(e) shows the PWM converter, it implies additional rectifier conduction losses and secondary parasitic ringing. Fig 1(f) shows the energy recovery snubber, the drawback of the circuit is the generation of additional losses and switching noise can be produced in the secondary side rectifiers.

This paper proposes a PSFB converter without circulating loss in primary side. Furthermore the voltage stress and current stress of the rectifier diode is reduced to a much low value compared with previous ZVZCS converter. The circuit diagram is shown in Fig 2. Here D1, D2 are main rectifier diodes. D_c is the clamping diode which is used to clamp the voltage spike across the rectifier diode. To implement the converter without an additional inductor, the leakage inductance of the transformer is utilized as the resonant inductor. In addition the proposed converter employs the voltage – doubler rectifier. In addition the resonance between the leakage inductor of the transformer and the rectifier capacitors can reduce the current stress of the rectifier diodes and conduction loses. Normally the voltage doubler is used in an ac–dc rectifier with the step up operation, and it is rarely adopted in dc–dc converters because of the voltage tolerance of the capacitor. However since the voltage doubler can behave as an inductance – capacitance filter, which eliminates the large output inductor. Due to the elimination of large output inductor, it features simple structure, lower cost, lighter weight and small mass. Further more, the proposed converter has wide zero-voltage switching ranges of lagging leg switches with low current stresses of the primary power switches by using the magnetizing current.

II. Operational Principle

The circuit diagram and key waveforms of the proposed converter are shown in figs 2 and 3 respectively. The operation of the proposed converter can be divided into twelve modes. One switching cycle of the proposed circuit is divided into two half cycles. 1. $t_0 - t_6$ and 2. $t_7 - t_{12}$. Since the operation principles of the two half cycles are symmetric, only the first half cycle is explained. One half cycle can be divided into six modes and its equivalent circuits are shown in fig.5.

A. Stage 1 (t_0~t_1)

At t_o M_4 turns on, the input V_{in} is across the transformer primary winding. The primary current I_p increases linearly until it reaches the reflected output inductor current as follows.

$$I_p(t) = \frac{1}{n}\left[\frac{V_{in}}{n} - V_{o1}(t_o)\right]\frac{1}{z_0}\sin\omega_r(t - t_0) + I_m(t - t_o) \quad (1)$$

where $\omega_r = \frac{n}{\sqrt{L_{lk}C_r}}$, $z_0 = \frac{1}{n}\sqrt{\frac{L_{lk}}{C_r}}$,

$$c_r = c_{01} + c_{02}$$

The magnetizing current, which also rises with the resonance between the magnetizing inductor and the rectifier capacitors, is obtained as follows.

$$I_p(t) = I_m(t_0)\cos\omega_m(t - t_0)\frac{nV_{o1}(t_o)}{Z_m}\sin\omega_m(t - t_0) \quad (2)$$

where $\omega_m = \frac{n}{\sqrt{L_m C_r}}$, $z_m = n\sqrt{\frac{Lm}{Cr}}$,

$$C_r = C_{o1} + C_{o2}$$

On the other hand, since the resonant frequency ($f_m = \frac{\omega_m}{2\pi}$) is much slower than the switching frequency, I_m can linearly be approximated as follows:

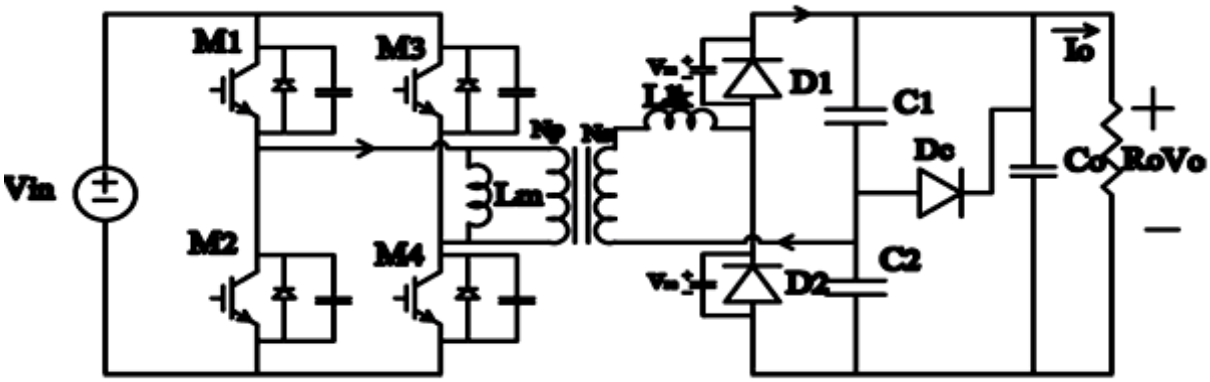

Fig. 2. Circuit Diagram of the proposed converter

$$I_m(t) = I_m(t_0) + \frac{nV_{o1}(t - t_o)}{L_m}(t - t_0) \quad (3)$$

B. Stage 2 (t_1~t_2)

At t_1 the leakage inductor of the transformer is resonant with the rectifier capacitors C_1, C_2. The equivalent circuit of

this interval is shown in Fig.5 (b). In order to calculate the magnitude of the resonant voltage and current, the equivalent circuit can be simplified into a resonant circuit as shown in fig.5. Where V_c *(t)* is the voltage across the rectifier capacitor. The voltage V_{rec} *(t)* = V_c*(t)*. This interval ends when the voltage increases to $(V_0 + V_{c1}) = 3V_0/2$

$$I_{LK} = I_0 + \frac{V_{in}/n - V_{c1}}{Z_r}\sin\omega_r(t - t_1) \qquad (4)$$

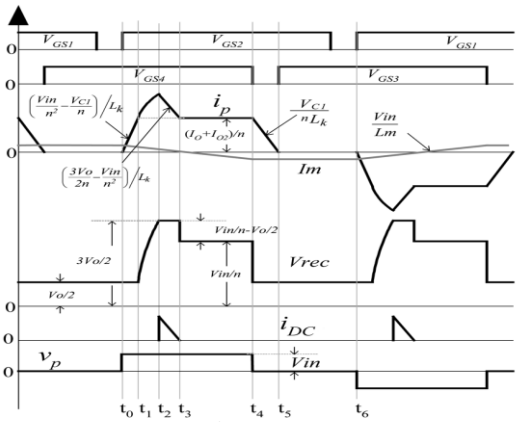

Fig. 3. Key waveforms in one switching cycle.

$$V_c(t) = \frac{V_{in}}{n}(1 - \cos\omega_r(t - t_1)) + V_{c1}\cos\omega_r(t - t_1) \qquad (5)$$

$$I_p(t) = I_{LK}(t)/n \qquad (6)$$

where $z_r = \sqrt{L_{lk}/c}$,

$$c = c_1 + c_2\ ,\ \omega_r = \frac{1}{\sqrt{L_{lk}C}}\ ,\ V_{c1} = V_0/2$$

C. Stage 3 ($t_2 \sim t_3$)

When the voltage V_{rec} reaches to $3V_0/2$, the clamping diode D_C conducts. Thus, the voltage V_{rec} is clamped to $3V_0/2$. The equivalent circuit of this stage is shown is Fig5(c). Because of reflected voltage V_{in}/ n from input is lower than $3V_0/2$ the current in L_{lk} begins decreasing at t_2. The voltage across L_{lk} is $[3V_0/2 - V_{in}/n]$. This stage ends when the current I_p decreases to

$$\frac{di_p}{dt} = \left(\frac{3V_0}{2n} - \frac{V_{in}}{n^2}\right)/L_{LK} \qquad (7)$$

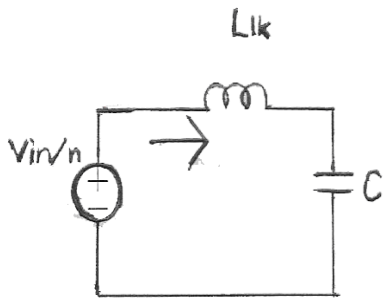

Fig. 4. Resonance circuit

D. Stage 4($t_3 \sim t_4$)

When D_C cut off V_{rec} keeps at V_{in}/n. The voltage spike across the rectifier diode is reduced.

E. Stage 5($t_4 \sim t_5$)

At t_5 , M_1 turns off. The intrinsic capacitors of M_1 and M_2 are charged by reflected load current. When voltage across M_1 reaches to V_{in}, the body diode of M_2 conducts. Thus, M_2 can achieve ZVS turning on. The voltage transition mode of lagging leg switches is similar to conventional PSFB converter. Furthermore, the voltage increases very fast because of large primary current reflected from load current. When the body diode of M_2 conducts, the voltage across primary winding is clamped to zero. Thus, the current in primary is begins decreasing, and the decreasing slope is described as follows. This interval ends when current i_p is reset to zero.

$$\frac{d_{ip}}{dt} = \frac{V_C}{n}\frac{1}{L_{lk}} \qquad (8)$$

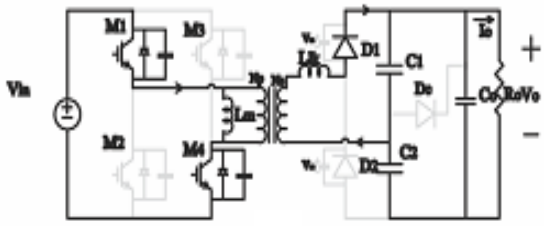

Fig. 5 (a). Equivalent circuit of stage 1 (t_0~t_1)

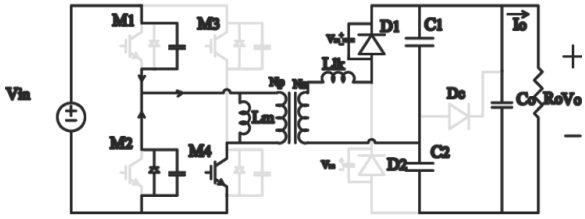

Fig. 5 (b). Equivalent circuit of stage 2 (t_1~t_2)

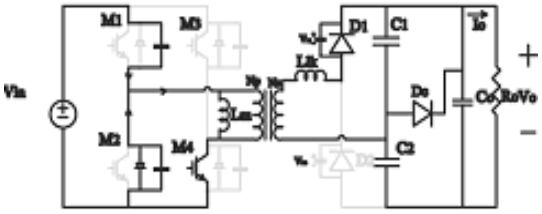

Fig. 5 (c). Equivalent circuit of stage 3 (t_2~t_3)

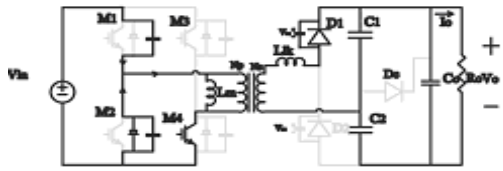

Fig. 5 (d). Equivalent circuit of stage 4 (t_3~t_4)

Fig. 5(e). Equivalent circuit of stage 5 (t_4~t_5).

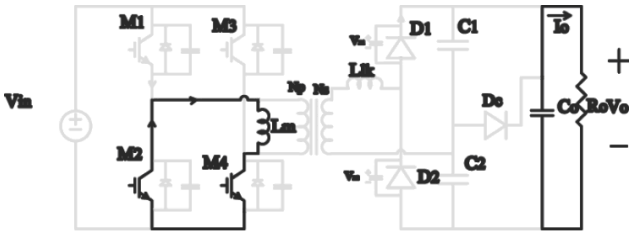

Fig. 5(f). Equivalent circuit of stage 6 (t_5~t_6)

F. Stage 6(t5 ~t6)

After t_5 the converter is in freewheeling stage. Because the primary circulating current is reset to zero, the circulating loss in primary side is eliminated without considering the transformer magnetizing current. Due to the clamping diode the voltage spike across the rectifier diode is eliminated. After t_5 the other half switching cycle begins. Due to the symmetry operation characteristics, the principles and the equivalent circuits of the other half switching cycle are same to that mentioned above.

III. Analysis of the Proposed Converter

A. ZVS and Circulating Energy

In the conventional PSFB converter the ZVS operation of the leading leg switches can easily be achieved due to the large output filter inductor. But due to large output inductance core loss occurs due to the saturation of core. This is eliminated with the help of the proposed converter: To implement the converter without additional inductance, the leakage inductance of the transformer is utilized as the resonant inductor. Due to its many advantages, including high efficiency, minimum number of devices, and low cost, this converter is attractive for high–voltage and high–power applications.

B. Reduction of Current stress and Conduction loss by using Resonance

A disadvantage of the proposed converter is that the current stresses of the rectifier diodes are rather large. This is because the proposed converter employs the voltage doubler, which causes the voltage - current doubling effects. However, the resonance between the leakage inductor and the rectifier capacitors reduces not only the current stresses of rectifier diodes but also conduction losses.

$$V_c(t) = \frac{V_{in}}{n}\left[1-\cos\omega_r(t-t_1)\right] + V_{c1}\cos\omega_r(t-t_1) \quad (9)$$

$$I_p(t) = I_{LK}(t)/n \quad (10)$$

where $\omega_r = \frac{1}{\sqrt{L_{lk}C}}$, $z_r = \sqrt{L_{lk}/c}$, $V_c = V_0/2$ (11)

C. Voltage stress of the Rectifier Diode

The auxiliary clamp diode is used to clamp the voltage spike across the rectifier diode, which releases the voltage stress of the rectifier diode.

D. Filter Requirements

The filter requirements of the proposed converter are different from that of conventional PSFB Converter because there is an auxiliary voltage source at the input of the filter inductors during the freewheeling interval. The current ripple (peak top peak) is derived according to different duty cycles.

$$I_{pp} = \frac{V_o}{4L_o}(1-D)T_s \quad (12)$$

The current ripple in function of input V_{in} is derived as

$$I_{pp} = \frac{V_o(V_{in}-nV_o)}{2L_o(2V_{in}-nV_o)}T_s \quad (13)$$

The ripple reduction in the proposed converter is about 60 - 80 % during the input voltage range compared with the conventional PSFB.

IV. Design Considerations

To validate the features of the proposed converter, a prototype converter has been designed using the following procedures, with the specifications that the input voltage V_{in} = 390~410V; the output voltage V_0 = 205 V and the switching frequency f_s = 60 Khz.

E. Selection of Resonant Frequency

To reduce the current stresses of rectifier diodes and conduction losses the resonant frequency, which is decided by the leakage inductance and the rectifier capacitance, should be selected using

$$c_{01} = c_{02} = \frac{n^2}{8\pi^2 L_{lk} f_{s^2}}\left[\frac{f_s}{f_r}\right]^2 \quad (14)$$

And Fig .6 after the leakage inductance is determined. To analyze the converter, two quantities are defined as frequency ratio.

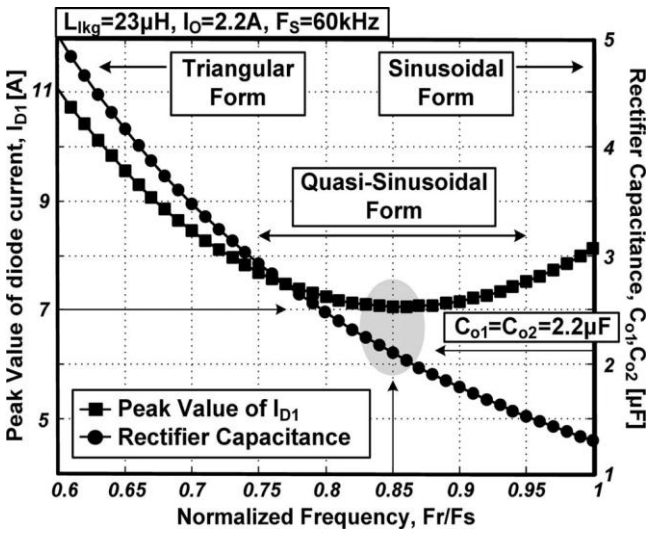

Fig. 6. Selection of resonant frequency.

$$F = \frac{f_r}{f_s} \quad (15)$$

And quality factor

$$Q = \frac{4\omega_r L_{lk}}{R_o} \tag{16}$$

F. Selection of Magnetizing Inductance and Dead Time.

The magnetizing inductance and dead time are the main factors of the ZVS of lagging leg switches such that they can properly be selected using

$$\Delta t_{dead} = C_0 \frac{V_{in}}{I_m(t_3)/2} \tag{17}$$

V. EXPERIMENTAL RESULTS

A 540 –W prototype of the proposed converter was built. The parameters of this prototype circuit are listed in table 1. Experimental waveforms are shown in Fig (7). As mentioned above due to the lack of output inductor the voltage stress across the rectifier is highly reduced, we can obtain high voltage without ringing. In addition with the help of leakage inductance of the transformer the circulating loss is eliminated. So during the freewheeling period, only a small magnetizing current is flowing through the primary side of the transformer. With the help of clamping diode the voltage stress across the rectifier diode is considerably reduced. The resonance between leakage inductance of the transformer and rectifier capacitor reduce the current stress, voltage spike of the rectifier diodes and conduction losses. Using voltage doubler circuit we can obtain high voltage without any additional circuits. From the experimental results we conclude that, this circuit is applicable for high voltage and high power applications

TABLE I: PARAMETERS OF THE PROTOTYPE CIRCUIT

Item	Symbol	Value /Part
Input voltage	V_{in}	390 ~ 410v
Output voltage	V_o	205V
Max. Power Rating	P_{max}	451V
Switching frequency	F_s	60KHz
Turns Ratio	n : l	3.23:1
Leakage inductance	L_{lk}	23 μ H
Magnetizing Inductance	L_m	1.4mH
Capacitance of double cell	C_1,C_2	2.2 μ F
Output capacitance	C_O	1000 μ F
Power switches	$M_{1\sim4}$	FQP12 N 60
Rectifier Diodes	$D_{1\sim2}$	15 ETH03

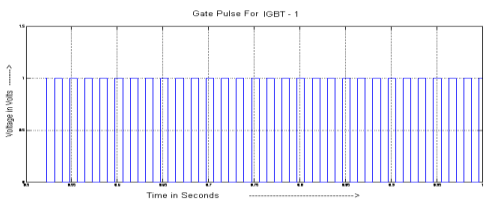

Fig. 7 (a). Gate pulse of S_1

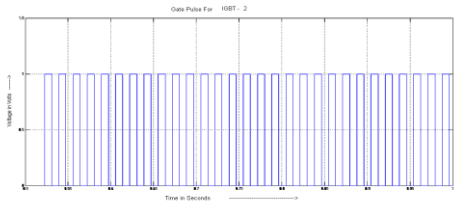

Fig. 7. (b) Gate pulse of S_2

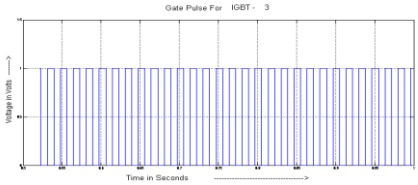

Fig. 7 (c). Gate pulse of S_3

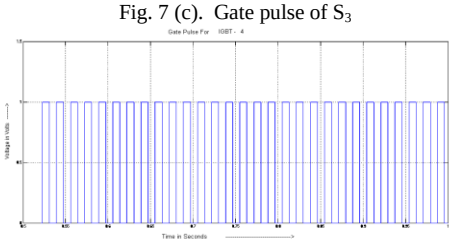

Fig. 7 (d). Gate pulse of S_4

Fig. 7. Experimental waveforms of the proposed converter

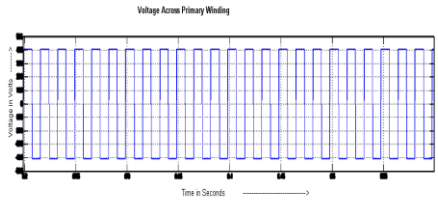

Fig. 7 (e). Voltage across primary winding

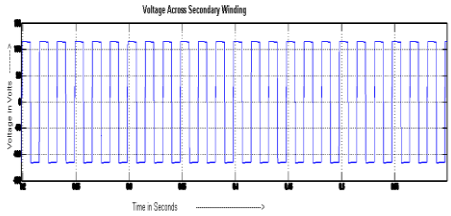

Fig. 7 (f). Voltage across secondary winding

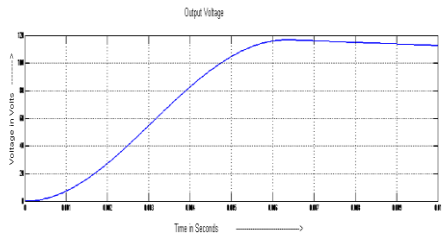

Fig. 7(g). Output voltage

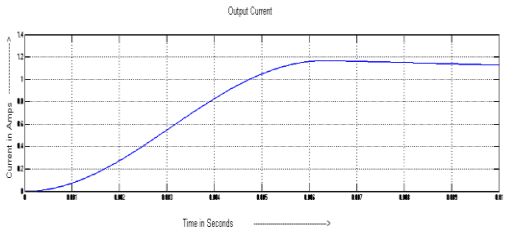

Fig. 7(h). Output current

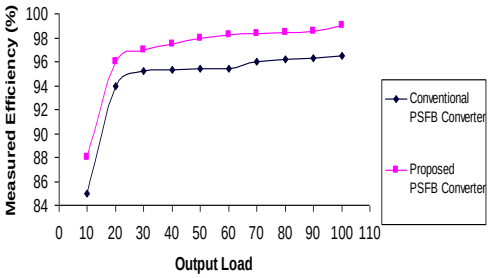

Fig. 8. Efficiency comparison under load variation

VI. Conclusion

A new soft switched full bridge converter with voltage doubler type rectifier is presented. By employing an auxiliary clamp diode the voltage stress across the rectifier diode is reduced, and low voltage rate diode can be utilized to reduce the conduction loss. Also the lead, lag switches achieves ZVS on. In addition since all energy that is stored in the leakage inductor of the transformer is transferred to the output side, the circulating energy is considerably reduced. A prototype has been used in the experiments to prove the validity of the proposed converter. The measured efficiency with wide load range, i.e., as high as around 98%, demonstrated higher efficiency than in conventional PSFB converters. Therefore, the improved efficiency of the proposed converter demonstrates it is suitable for high voltage and high power applications.

References

[1] X. Rual and Y. Yan, "A novel Zero Voltage and Zero Current Switching PWM Full Bridge Converter Using two Diodes in series with the lagging leg," *IEEE Trans Ind.* Electron, vol. 48, no. 4, pp.777-78, 2001.

[2] W. Li, Y. Shen, Y. Deng, and X. He, "A ZVZCS full-bridge dc/ac converter with a passive auxiliary circuit in the primary side," in *Proc. IEEE PESC*, pp. 2305-1140, 2006.

[3] J. Dudrik, P. Spanik, and N. D. Trip, "Zero-voltage and zero current switching full bridge dc-dc converter with auxilary transformer," *IEEE Trans.Power* Electron., vol. 21, no. 5, pp. 1328-1335, 2006.

[4] T. F. Cheng and S. Cheng, "A novel zero-voltage zero current switching full bridge PWM converter using improved secondary active clamp," in *Proc. IEEE ISIE*, pp.1683-1687, 2006.

[5] J. G. Cho, J. Sabate, G. Hua, and F. C. Lee, "Zero voltage and zero current switching full bridge PWM converter for high power applications," *IEEE Trans. Power Electron*, vol. 11, pp. 622-628, 1966.

[6] H. J. Chiu and L.W. Lin, "A high – efficiency soft – switched AC/DC converter with current–doubler synchronous rectification," *IEEE Trans. Ind. Electron*, vol. 52. no. 3, pp. 709-718, 2005.

[7] J. Y. Lee, "An improved magnetic – coupled AC-PDP sustain drive with dual recovery paths," *IEEE Trans. Ind. Electron*, vol. 54, no. 3, pp. 1623 – 1631, 2007.

[8] E. H. Kim and B. H. Kwon, "Zero voltage and zero current switching Full-Bridge converter with secondary resonance," *IEEE Transactions on industrial Electronics*, vol. 57, no. 3, 2010.

[9] S.Y. Lin and C. L Chen, "Analysis and design for RCD clamped snubber used in output rectifier of phase–shift full–bridge ZVS converters," *IEEE Trans. Ind. Electron*, vol. 45, no. 2, pp. 358 -359, 1998.

V. Delbin Jelaja received her B.E degree in Electrical and Electronics Engineering from C.S.I Institute of Technology, Thovalai, Tamil Nadu India, in 2003 and thereafter, she did her M.E. degree in Power Electronics and Drives from Government Engineering College, Tirunelveli, Tamil Nadu, India in the year 2009. She is presently a research Scholar at Anna University. Her area of interest is Electrical Engineering, Power Electronics, which includes soft switching in electric vehicles and high power Applications.

M. Rajaram, Vice Chancellor Anna University of Technology, Tirunelveli, Tamil Nadu, India. He completed his B.E. Degree (Electrical and Electronics Engineering) at Alagappa Chettiar College of Engineering and Technology, Karaikudi in 1981, M.E. Degree (Power Systems) at Government College of Technology, Coimbatore, in 1988 and Ph.D (Control Systems) at PSG College of Technology, Coimbatore in 1994. He has successfully supervised 11 Ph.D and M.S (by Research) Scholars who are awarded with the Doctoral Degree and 10 candidates are pursuing Ph.D under his guideship at present. To his record he has published his Research findings in 75 International Journal/National Journals, 61 International Conferences and 53 National Conferences. He has also authored 6 Text Books, which the Engineering students find informative and useful. He is a life member of ISTE and MIE and an AICTE Expert member and the Chairman in granting affiliation to Engineering Colleges and Polytechnics.