

Design and Analysis of a Compact Reversible Ternary Systolic Array

Naushin Nower and Ahsan Raja Chowdhury

Abstract—Multi-valued logic synthesis is a very promising and affluent research area at present because of allowing designers to build much more efficient computers than the existing classical ones. In this regard, research on ternary logic synthesis has got impetus in the recent years. Many existing literature are mainly perceptive to the realization of efficient ternary reversible processors. This research is based on the design of a reversible systolic array, one of the best examples of the parallel processing, using micro level ternary Toffoli gate. General architecture of the ternary reversible systolic array multiplier is shown along with example. Lower bound for the quantum cost and the garbage outputs in terms of entire circuit entire circuit is calculated here to establish the compactness of the design. Finally, comparative result shown that the proposed circuit outperforms the existing one both in terms of number of gates and Quantum cost analysis.

Index Terms—Fuzzy logic, garbage output, systolic array, quantum cost.

I. INTRODUCTION

In digital design, energy loss plays a significant role. Energy dissipation is associated to non-identity of switches and materials. It has been proved that, irreversible logic computation generate $kT\ln 2$ heat for every bit that is lost (where k is the Boltzmann's constant and T is the temperature) [1, 2]. Though for a room temperature T , the amount of dissipating heat is minuscule (i.e. 2.9×10^{-21} joules) but not negligible. The design that doesn't resulting information loss called reversible, which is emerging as a flourishing area of research due to its' applications in different sectors such as quantum computing, nanotechnology, and optical computing etc. Moreover, systems that perform operations in a reversible fashion can dissipate less energy and might prove competitive today. Reversible are circuits (gates) in which the number of inputs is equal to the number of outputs and there is a one-to-one mapping between vectors of inputs and outputs; thus the vector of input states can always be re-constructed from the vector of output states [2]. More formally, a reversible logic gate is a k -input, k -output (denoted $k*k$) device that maps each possible input pattern into a unique output pattern [2]. This fact is also applicable for multiple-valued logic, which demonstrates several potential advantages over binary technology. Quantum technology is inherently reversible

and one of the most potential technologies for future computing systems [3].

Ternary logic synthesis research provides a new-fangled era at present. Syntheses on ternary quantum logic using basic 2-qutrit controlled gates are presented on [4, 5]. The major sub-circuit needed for ternary logic has already been proposed in many literatures. Practically important ternary circuits like adder, subtractor, encoder, decoder, multiplexer, demultiplexer, comparators has already been proposed and currently been revising in many literatures. Realization of ternary reversible/quantum adder/subtractor is given in [5]. Synthesis of ternary reversible/quantum encoder and decoder is given in [6]. Realization of ternary reversible/quantum multiplexer/demultiplexer is given in [7].

In this paper, we present a design of reversible/quantum realization of ternary systolic array which is first proposed in literature. The design is based on Toffoli gates and 2-qutrit Muthukrishnan-Stroud (M-S) gates [8]. Systolic array [9] is a specialized form of parallel computing. A systolic array formed by interconnecting a set of identical data-processing cells in a uniform manner is a combination of an algorithm and a circuit that implements it, which is closely related conceptually to arithmetic pipeline. First ever Systolic Array in Reversible mode was proposed in [10], but that was based on Fuzzy Logic and Fuzzy Theory.

The rest of the paper is organized as follows: Section II provides the necessary background on reversible logic along with the examples of some popular reversible gates. Section III shows the details of existing Systolic array, whereas the proposed design technique for Reversible Ternary Systolic Array is presented in Section IV. Evaluation of the proposed design and Comparative Study is presented in Section V. The paper concludes in Chapter VI. Some important references are listed in Section VII.

II. BASIC DEFINITION LITERATURE REVIEW

In this section introduces some basic terms and definitions used in this paper and some outcome of previous researchers.

A. Ternary Quantum Logic

A ternary, three-valued or trivalent, logic is the simplest introduction of multi-valued logic which is also referred to as 3VL. To define ternary logic let $A = \{0, 1, 2\}$. A ternary logic circuit f with n input variables, A_1, \dots, A_n , and n output variables, P_1, \dots, P_n , is denoted by $f : A^n \rightarrow A^n$, where $(A_1, \dots, A_n) \in A^n$ is the input vector and $(P_1, \dots, P_n) \rightarrow A^n$ is the output vector. There are 3^n different assignments for the input vectors. A ternary logic circuit f is reversible if it is a one-to-one and onto function (bijection). A ternary reversible logic circuit with n inputs and n outputs

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is also called an n -qudit ternary reversible gate.

In the ternary quantum logic system the unit of memory (information) is a qutrit (quantum ternary digit) and the ternary logic values (0, 1, and 2) are represented by a set of distinguishable different states of an object that represent the qutrit. After encoding these distinguishable quantities into ternary constants, qutrit states are represented by $|0\rangle$, $|1\rangle$ and $|2\rangle$ respectively, and are called the computational basis states [5].

B. Ternary Galois Field Logic

Ternary Galois Field (TGF) consists of the set of elements $T = \{0, 1, 2\}$ and two basic binary operations—addition (denoted by $+$) and multiplication (denoted by \cdot or absence of any operator) as defined in Table I. GF3 addition and multiplication are closed, i.e., for $x, y \in T$, $x + y \in T$ and $xy \in T$. GF3 addition and multiplication are also commutative and associative, i.e., $x + y = y + x$ and $xy = yx$ (commutative), and $x + (y + z) = (y + z) + x = z + x + y$ and $x(yz) = (xy)z$ (associative). GF3 multiplication is distributive over addition, i.e. $x(y + z) = xy + xz$

TABLE I. TERNARY GALOIS FIELD (GF3) OPERATIONS

+	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

●	0	1	2
0	0	0	0
1	0	1	2
2	0	2	1

C. Ternary Muthukrishnan-Stroud Gate

Muthukrishnan and Stroud proposed a family of 2-qudit (quantum digit) d -valued gates [8], which applies a 1-qudit unitary transform on the second qudit conditional on the first qudit being $(d - 1)$. The ternary M-S gate is a controlled gate [8] where the input A is the controlling input and the input B is the controlled input. The output P is equal to the input A . The output Q is the Z transform of the controlled input B if the controlling input $A = 2$, Q is equal to B otherwise. The ternary M-S gates can be realized using liquid ion trap quantum technology as an elementary gate [8]. Therefore, we assign these gates a cost of 1.

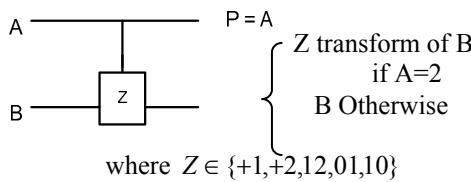


Fig. 1. Symbol of M-S gate

D. Quantum Cost

Calculating Quantum cost of reversible circuit is a significant one. Every reversible gate can be calculated in terms of quantum cost and hence the reversible circuits can be measured in terms of quantum cost. Reducing the quantum cost from reversible circuit is always a challenging

one and works are still going on in this area. In this paper we will show the quantum equivalent diagram of reversible gate that will be used to calculate the final quantum cost of proposed reversible ternary Systolic Array.

E. Ternary Toffoli Gate

Ternary Toffoli gate is shown in Fig. 2(a), where its' corresponding MS implementation is shown in Fig. 2(b). If the two controlling input values are 2, then Z transform is applied on controlled input otherwise controlled input is passed unchanged. That is the outputs of the gate are $P = A$, $Q = B$, and $R = Z$ transform of C if $A = 2 \wedge B = 2$, where $Z \in \{+1, +2, 12, 01, 10\}$; $C = Q$ otherwise.

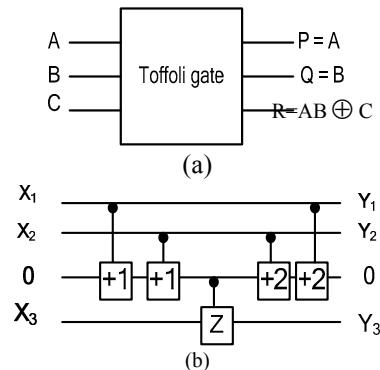


Fig. 2. 3-Qutrit ternary Toffoli gate: (a) Toffoli gate with I/O mapping (b) realization using M-S gates

Realization of this gate using M-S gates is shown in Fig. 2(b), where a constant input 0 is changed to 2 by using two +1 transforms controlled from the two controlling inputs A and B , and then the resultant constant 2 is used to control the input C [6]. The right most two gates are the inverse gates of the left most two gates used to restore the constant input 0. The quantum cost of this realization is 5.

F. Garbage Output

Every gate output that is not used as input to other gate or as a primary output is called garbage. The unutilized outputs from a gate are called “garbage”. Heavy price is paid off for every garbage output. Suppose we want to find the Ex-OR between two variables in reversible computation, then the circuit will look like Fig. 3. One extra output should be produced to make the circuit reversible and that unwanted output ($P=A$, marked as *) is known as garbage.

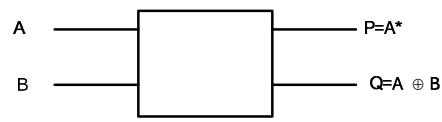


Fig. 3. The garbage output A*

III. EXISTING DESIGN OF SYSTOLIC ARRAY

Ali, Chowdhury and Babu, proposed a reversible systolic array [10] that can operate in Fuzzy mode. In that paper [10], authors described the composition of fuzzy relations along with the systolic array structure to compute it. Collections of fuzzy *if-then* rules or fuzzy algorithms are mathematically equivalent to *fuzzy relations* and the problem of inference of (evaluating them with specific values) is mathematically equivalent to the composition of [2], [4].

In fuzzy set theory and fuzzy logic the min and max operations are the most significant and frequently used one.

In [10], authors have considered the membership-values to be digitized and representable in 2 ternary variable. Consider the calculation of $\min(X, Y)$, where X and Y are 3 bit membership values. It is seen that $X > Y$ when $X + Y$ produces a carry of 1 and then $\min(X, Y) = Y$. On the other hand if no carry is produced then $\min(X, Y) = X$ i.e. the values can be passed to the output. It can be pointed out that if the membership-values are equal then either X or Y can be passed to the output of the circuit. The max operations are just the opposite. Fig. 4 shows the design of a fuzzy cell in reversible mode which is composed of 4 Multiple Valued Fredkin gates. In the first stage of Fig. 4, the carry generates $g_i = a_i b_i$ and carry propagates $pi = a_i \text{EXOR} b_i$ are generated and they are combined to produce c_{out} . Depending on the c_{out} , in the last stage, Either X or Y is passed to the output. By using this max-min cell they realize the fuzzy systolic array and calculate the gate and garbage cost.

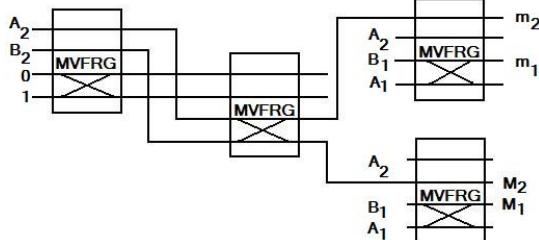


Fig. 4. Single cell of a Systolic Array using four Multiple Valued Fredkin Gates

According to [10] n-bit MAX/MIN cell of a systolic array can be realized with at least $4n$ reversible gates. To multiply 2 matrixes with dimension $p \times m$ and $m \times r$, we need a systolic array with $p \times (2r-1)$ cells.

So in Fuzzy Reversible Systolic Array we need total= $4n \times [p \times (2r-1)]$ gate.

If n is the no. of bits in a MAX/MIN cell of a systolic array and Q is the quantum cost required to realize the cell, then

$$Q \geq 4Q_{FRG} \quad (1)$$

where, Q_{FRG} is the quantum cost of Fredkin gate.

We need a systolic array with $p \times (2r-1)$ cells to multiply 2 matrixes with dimension $p \times m$ and $m \times r$. And in Fuzzy Reversible Systolic Array we need total= $4n \times [p \times (2r-1)]$ gate. Each gate (Max-Min cell) has a Quantum cost $Q \geq 4Q_{FRG}$. So total quantum cost for calculation of 2 matrixes with dimension $p \times m$ and $m \times r$ is

$$\begin{aligned} & 4Q_{FRG} \times (4n \times [p \times (2r-1)]) \\ & = 16 \times Q_{FRG} \times n \times ([p \times (2r-1)]) \end{aligned} \quad (2)$$

IV. REALIZATION OF TERNARY SYSTOLIC ARRAY: THE PROPOSED DESIGN

Systolic array [9] is a specialized form of parallel computing. A systolic array formed by interconnecting a set of identical data-processing cells in a uniform manner is a combination of an algorithm and a circuit that implements it, and is closely related conceptually to arithmetic pipeline. In a systolic array, data words flow from external memory in a

rhythmic fashion, passing through many cells before the results emerge from the array's boundary cell and return to external memory. The external memory connected to the systolic array's boundary cell stores both input data and results. Upon receiving data words, each cell performs same operation and transmits the intermediate results and data words to adjacent cells synchronously. The underlying principle of systolic array is used to achieve massive parallelism with a minimum communication overhead. The basic functional unit of a systolic array is cell which act as an autonomous processor. Cells (processors) compute data and store it independently of each other.

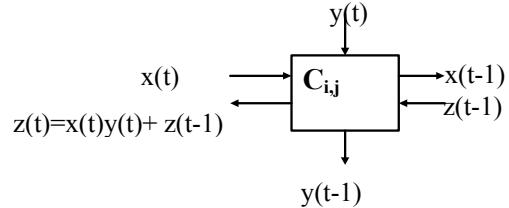


Fig. 5. Systolic array cell structure

The Fig. 5 demonstrates the elementary cell structure. The distinguish features of reversible systolic array have been discussed in many literature. The authors of the paper [10] have been illustrated the composition of fuzzy relations and describe a systolic array structure to compute that fuzzy relations on binary logic. But this paper provides a realization of ternary systolic array using M-S gate which is not introduced in any other literature in precedent. Our previous contributions towards Reversible Ternary Systolic Array [11, 12] only highlight the abstract design idea, but this paper shows a step by step design methodology the design along with theoretical underpinning and comparative study.

In this research, each cell is intended to perform as a ternary systolic array operation. The function of proposed ternary systolic array processor is to execute the multiplication in pipeline fashion, which is represented by following equations:

$$\left. \begin{aligned} z(t) &= z(t-1) + x(t).y(t) \\ x(t) &= (x_{n-1}, x_{n-2}, \dots, x_0) \\ y(t) &= (y_{n-1}, y_{n-2}, \dots, y_0) \end{aligned} \right\} \quad (3)$$

where, x is the multiplicand with n trits, y is the multiplier with n trits.

Ternary form of this equation becomes:

$$z(t) = (((a(t)b(t)) \bmod 3 + z(t-1)) \bmod 3 \quad (4a)$$

$$z(t) = (z(t-1) + a(t) \times b(t)) \bmod 3 \quad (4b)$$

First one is used for generating ternary performance of systolic array. From the first equation the subsequent Table II is generated.

By observing the truth table closely, we find that we can formulate Ternary Toffoli Gate as a single cell of the proposed Reversible Ternary Systolic Array. For clarity, truth table for Ternary Toffoli Gate is shown in Table III. After designing the cell, the full architecture can be realized using the same method of any conventional systolic array.

Consider an example of 2×2 matrix multiplication.

$$X = \begin{vmatrix} 1(x_{11}) & 2(x_{12}) \\ 2(x_{21}) & 1(x_{22}) \end{vmatrix} \quad Y = \begin{vmatrix} 1(y_{11}) & 1(y_{12}) \\ 0(y_{21}) & 2(y_{22}) \end{vmatrix}$$

So, their resultant product is

$$Z = \begin{vmatrix} 1(z_{11}) & 2(z_{12}) \\ 2(z_{21}) & 1(z_{22}) \end{vmatrix}$$

$$\text{where } z_{11} = x_{11} \times y_{11} + x_{12} \times y_{21}$$

$$z_{12} = x_{11} \times y_{12} + x_{12} \times y_{22}$$

And z_{21} and z_{22} is calculated by the same way.

TABLE II. TRUTH TABLE FOR TERNARY SYSTOLIC ARRAY

a	b	(a*b) mod 3	z(t-1)	z(t)
0	0	0	0	0
0	0	0	1	1
0	0	0	2	2
0	1	0	0	0
0	1	0	1	1
0	1	0	2	2
0	2	0	0	0
0	2	0	1	1
0	2	0	2	2
1	0	0	0	0
1	0	0	1	1
1	0	0	2	2
1	1	1	0	1
1	1	1	1	2
1	1	1	2	0
1	2	2	0	2
1	2	2	1	0
1	2	2	2	1
2	0	0	0	0
2	0	0	1	1
2	0	0	2	2
2	1	2	0	2
2	1	2	1	0
2	1	2	2	1
2	2	1	0	1
2	2	1	1	2
2	2	1	2	0

$$\text{where } z(t) = ((a*b) \text{ mod } 3 + z(t-1)) \text{ mod } 3$$

TABLE III. TRUTH TABLE FOR TERNARY TOFFOLI GATE

C\AB	00	01	02	10	11	12	20	21	22
0	0	0	0	0	1	2	0	2	1
1	1	1	1	1	2	0	1	0	2
2	2	2	2	2	0	1	2	1	0

V. EVALUATION OF THE PROPOSED DESIGN AND COMPARATIVE STUDY

In this section, first we evaluate the proposed design with a Theorem and Lemma, followed by examples. After that, a comparative result is shown that proves the supremacy of the proposed design.

Theorem 1 Let, the dimension of two matrixes to perform systolic array are $n \times m$ and $m \times r$. If T_{GB} is the total number of garbage output generated to the realized systolic array then

$$T_{GB} \geq (2n-1) \times (2n+2r-1) + (p-(2n-1)) \times (2n+2r-2)$$

where, p = total number of needed cycle.

Proof: To multiply 2 matrixes with dimension $n \times m$ and $m \times r$, we need a systolic array with $n \times (2r-1)$ cells.

$$\text{Let } p \text{ (the number of needed cycle)} = n \times (2r-1) - 2$$

$$Q \text{ denotes the total output} = n \times r$$

T_{GB} denote the total number of garbage output generated by the systolic array.

If we consider a systolic array, we can observe that we get garbage output from three sides of a systolic structure. The side boundaries can denote by

$$G_L = \text{left boundary} = n$$

$$G_B = \text{below/down/bottom boundary} = 2r-1$$

$$G_R = \text{right boundary} = n$$

The upper side of a systolic array is only restricted for to provide inputs.

Now consider the 1st cycle of a systolic array. In the case of 1st cycle the number of garbage output = $(n+2r-1+n)$.

From the observation we see that up to $(2n-1)$ cycle the total garbage produced = $(2n-1) \times (n+2r-1+n)$. Apart from first $(2n-1)$ cycle the number of garbage output produced by the other cycle = $(p-(2n-1)) \times (n+2r-1+n-1)$.

So total number of garbage output produced by the systolic array

$$T_{GB} \geq (2n-1) \times (n+2r-1+n) + (p-(2n-1)) \times (n+2r-1+n-1)$$

$$T_{GB} \geq (2n-1) \times (2n+2r-1) + (p-(2n-1)) \times (2n+2r-2)$$

Example 1: Consider an example of two 2×2 matrix multiplication. Initial state of the corresponding architecture is shown in Fig. 6. In this case the number of garbage output produced by 1st cycle is $(n+2r-1+n) = (2 \times (2 \times 2 - 1) + 2 = 2 + 3 + 2 = 7)$. Up to $(2n-1)$ cycle the garbage output is 7. That is for 2×2 matrix multiplication up to 3 cycles the produced garbage is 7. From the Fig. 7 we see that the $x_{11} \times y_{11}$ is produced at 2nd cycle and it appear as an output at 4th cycle (as in Fig. 8). Output of the 2nd cycle is shown in Fig. 8. The first output we get at 4th cycle which is shown in Fig. 9.

So up to 3rd cycle we get total 7 garbage output. After $(p-(2n-1))$ that is, from the 4th cycle we get output from each of the left side boundary cell alternatively. From the 4th cycle to p^{th} cycle the garbage output will be $(n+2r-1+n-1)=6$.

Lemma 1: The quantum cost of a systolic array, using each cell as a Toffoli gate is $5 \times C$, where, C is the number of cell used in a systolic array.

Proof: As we know each quantum gate operates by manipulating qubits and quantum cost is associated with qubits [3]. The proposed systolic array is implemented by using 3 qubit ternary Toffoli gate as a cell. The quantum cost of the used cell realization is 5. Hence, if the number of cell required in a systolic array is C , the total quantum cost of the proposed realization is $5 \times C$.

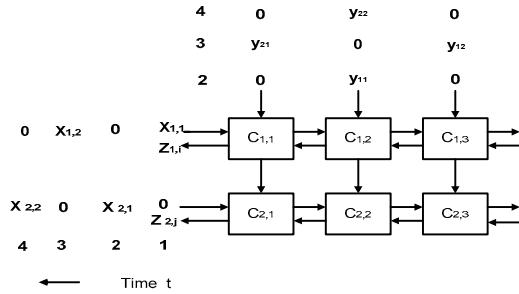


Fig. 6. Systolic array for 2×2 matrix multiplication

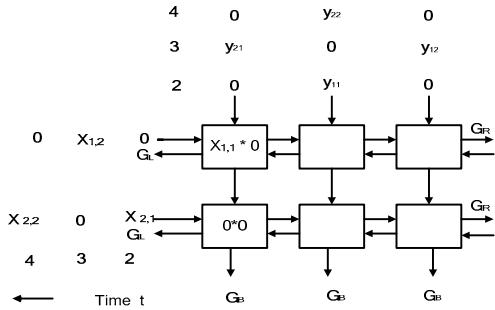


Fig. 7. The garbage output produced at 1st cycle

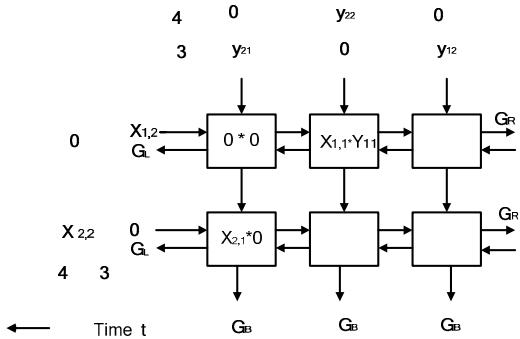


Fig. 8. The garbage output produced at 2nd cycle

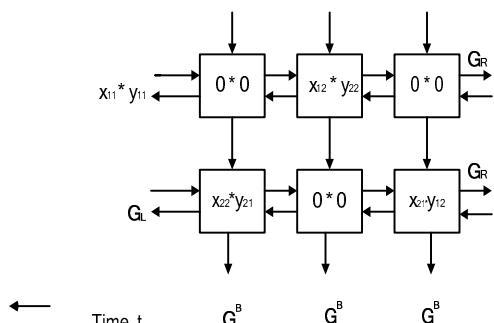


Fig. 9. First output ($x_{11} * y_{11}$) produced at 4th cycle

A comparative study result is shown in Table IV which clearly shows the superiority of the proposed design.

Though the garbage of the proposed design seems to be higher than the existing design, proposed design performs better in other two parameters.

TABLE IV. COMPARATIVE STUDY BETWEEN PROPOSED METHOD AND [10]

Comparison Parameter	Reversible Fuzzy Systolic Array [10]	Ternary Reversible Systolic Array (Proposed)
Number of Gates	$4nC$	C
Quantum Cost	$16 \times Q_{FRG} \times n \times C$	$5C$
Number of Garbage Outputs	$4 \times n \times C$	$D \times (C+D+1)+(p-D) \times (C+D)$

where $C = p \times (2r-1)$, $D = (2n-1)$

VI. CONCLUSION

In this paper, we present the realization of ternary reversible systolic array. We have developed the proposed architecture with the aid of Toffoli gate. Lower bound for Garbage output is developed very significantly to evaluate the proposed design. We have compared the proposed design with the existing one in terms of garbage outputs and quantum cost. From the comparative study it can be easily understandable that proposed method performs better in terms of Quantum Cost analysis and Number of gate count.

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