Design Considerations of Electrically Induced Source/Drain Junction SOI MOSFETs for the Reduced Short Channel and Hot Carrier Effects

Santosh Kumar Gupta and S. Baishya

Abstract—Due to scaling of the channel length, SCEs and HCEs are becoming serious issues. To reduce these effects, electrically induced ultra-shallow source/drain junctions has been investigated using actual (Gaussian) source/drain doping profiles. In this paper the novel attributes of nano scale SOI MOSFETs with electrically induced source/drain junctions are presented with extensive simulation study. It has been found that the use of induced source/drain junctions is capable of controlling the short channel effects.

Index Terms—Electrically induced source/drain junctions, hot electron effect, short channel effects, silicon-on-Insulator.

I. INTRODUCTION

SOI has been in use by many leading manufacturers in the last decade due to the reasons it provide higher density, no substrate leakage current, resistance to latch-up, higher speed, reduced parasitic capacitance and thereby improving performance. But these devices suffer from the hot electron effect which increases the gate leakage current [1].

Due to the scaling of the channel length, short channel effects such as the threshold voltage roll off due to charge sharing between drain/source and channel, Drain Induced Barrier Lowering (DIBL) due to the variation of the source/channel barrier by the drain voltage and hence an increase in the OFF state leakage current. Therefore reduction of hot electron and short channel effects plays major role in scaling the SOI MOS devices. There have been many possible solutions proposed in the literature [2, 3, 4, 5, 6, 7, 8]. To reduce the hot electron and short channel effects ultra shallow extended source/drain has been proposed [9], but it is very difficult to fabricate ultra shallow junctions by conventional methods [10]. [11]

II. ELECTRICALLY INDUCED SOURCE/RAIN JUNCTION SOI (EJ-SOI) MOSFET STRUCTURE

A schematic cross sectional view of the Electrically Induced Source/Drain SOI MOSFET implemented using Sentaurus Structure Editor (SentaurusSE) and simulated with Sentaurus Device (SentaurusD) is shown in Fig. 1. The extremely shallow junctions are realized using triple gate structure with one main gate and two side gates with different

work functions (4.9 eV for the main gate and 4.7 eV for the side gates). The main gate can be biased separately than the two side gates. The doping level of the Source and Drain has been taken to have Gaussian profile with peak concentration (Arsenic) $1 \times 10^{20} \text{ cm}^{-3}$ at 10 nm with decrease in concentration to $5 \times 10^{17} \text{ cm}^{-3}$ at a depth of 25 nm and a spreading factor of 0.8 as shown in Fig. 2. This has been taken due to the fact that the actual implant process is Gaussian-like distribution and hence it cannot be modeled correctly with the uniform doping models.

The length of the main gate and side gates are respectively L_M and L_S . Silicon dioxide has been used as gate oxide and diffusion barrier between the gates. The thickness of the diffusion barrier has been chosen ($t_d = 2 \text{ nm}$) to be significantly smaller than the main and side gate lengths, and can't be taken smaller in size than the gate oxide. If one chooses thicker t_d then it will create a discontinuity between main and side gate regions in the channel [3]. The channel is uniformly doped with a constant concentration (Boron) of $6 \times 10^{16} \text{ cm}^{-3}$.

Since the thermal equilibrium approximation is not valid for the SOI MOSFETs [3], Hydrodynamic model (full energy balance) has been used in our simulations. As in some devices the electric field in the direction of current flow is so high so as the carrier (electron/hole) velocity in the entire channel remains in saturation and hence carrier temperatures may vary significantly from the lattice temperature. SRH recombination model has been used to take into account the carrier generations in space charge regions and recombination in high injection regions. The doping and electric field dependent mobility models have been used in our simulations.

III. RESULTS AND DISCUSSIONS

In Fig. 3 the Sentaurus Device [12] simulated surface potential profiles of the Electrically Induced Source/Drain junctions SOI (EJ-SOI) MOSFET with the main gate length L_M (50 nm) and side gate lengths of L_S (50 nm) for a main gate voltage of 0.0 V and side gate voltages of 1.5 V has been compared with a 50 nm gate length, conventional SOI (C-SOI) MOSFET. As can be observed in the Fig. 3, there is no major change in the surface potential under the main gate due to variations in V_{DS} . It means that the main channel potential is “screened” from the drain voltage changes and hence there will be less threshold voltage roll-off due to drain voltage variations.

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The authors are with National Institute of Technology, Silchar, Assam - 788010 INDIA (email: santoshty@gmail.com).

Fig. 1. Cross-sectional view of the simulated EJ-SOI.

Fig. 2. Doping profile used in the Source/Drain for the EJ-SOI MOS transistor.

 Fig. 3. Comparison of surface potential in the channel region of EJ-SOI with that of C-SOI. the potential under the main gate is "screened" of variations in V_{DS} thereby reducing the short channel effects.

Fig. 4. Comparison of electric field in the direction of the current flow between EJ-SOI and C-SOI.

In Fig. 4 the electric field variations along the channel are shown for both the EJ-SOI ($L_M = 50$ nm) and C-SOI ($L_G = 50$ nm) with $V_{GS} = 0$ V. From the Fig. 4, it is clear that peak electric field has decreased at the drain end due to the presence of the extremely shallow inversion layer due to the

side gate potentials. Due to this the hot carrier effect, gate tunneling, and impact ionization near the drain end decreases. Due to smaller electric field near the drain side, breakdown voltage of the device improves whereas this is also going to decrease the electron velocity near the drain end.

Fig. 5. Comparison of output characteristics of EJ-SOI with C-SOI.

Output characteristics (I_D - V_{DS} curve) are shown in the Fig. 5. The conduction band energy and the electron density in the channel have been compared for both EJ-SOI and C-SOI in Fig. 6 and Fig. 7. The side gate length and bias has been optimized with extensive simulations and it was found that when $L_M = L_S$ it gives better characteristics as compared to other values.

Fig. 8 shows the variation of the surface potential on the side gate bias with main gate fixed at 1.5 V. Surface electron mobility and electric field have been compared for different side gate voltages in Fig. 9 and Fig. 10 respectively with $V_{DS} = 0$ V and $V_{MGS} = 1.5$ V. It can be observed that the mobility of electron is higher at 0.0 V side gate voltages and it decreases as the side gate voltage is increased due to the increase in the normal electric field. The 2D electric field variation is shown in the Fig. 11 for both EJ-SOI and C-SOI for the case when $V_{DS} = 0$ V and $V_{MGS} = 1.5$ V.

Fig. 6. Conduction band energy comparison of EJ-SOI with C-SOI.

Fig. 7. Comparison of electron density in the channel region of the EJ-SOI with C-SOI at different drain voltages.

Fig. 8. Surface potential in the channel of EJ-SOI for different side gate voltages.

Fig. 9. Surface electron mobility in the channel of EJ-SOI for different side gate voltages.

Fig. 10. Surface electric field in the channel of EJ-SOI for different side gate voltages.

Fig. 11 2D Variations of electric field in the channel of (a) EJ-SOI and (b) C-SOI.

Fig. 12. Comparison of electron temperature at the surface of the silicon thin layer in the EJ-SOI and C-SOI.

Fig. 13. Comparison of electron density at the surface of the silicon thin layer in the EJ-SOI and C-SOI.

In Fig. 12 the surface electron temperature in the channel region has been compared for both the EJ-SOI and C-SOI MOSFETs. It is observed that as the side gate length is increased (for the same main gate length as for C-SOI, $L_G=50$ nm) and similar bias conditions, the electron temperature also comes down which means that the hot electron effect has reduced significantly. The electron temperature is lower even when the side gate length comes down the main gate length. Whereas in C-SOI MOSFET case the electron temperature is significantly higher than the EJ-SOI MOSFET for the same channel length. This shows that the EJ-SOI is effective in reducing the hot electron effect.

Fig. 13 and 14 show the electron density and electron velocity respectively in the channel for both the cases. It can be observed that the electron velocity has improved for the case of EJ-SOI than the C-SOI.

Fig. 14. Comparison of electron velocity at the surface of the silicon thin layer in the EJ-SOI and C-SOI.

IV. CONCLUSION

Using 2-D simulations the design considerations for reduced short channel effects has been investigated for the EJ-SOI MOSFETs. It has been found that these transistors

are able to effectively reduce the short channel effects and the hot carrier effect as compared to the conventional SOI transistors. The hot carrier effects are reduced with the increase of side gate lengths. Besides the fact that there is an area penalty for the EJ-SOI MOSFETs as compared to the C-SOI MOSFETs; the EJ-SOI has many advantages over the latter. Considering all above facts it is concluded that EJ-SOI MOSFETs with same side and main gate lengths can be used to overcome the short channel effects (SCEs) and hot carrier effects (HCEs) effectively.

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Santosh Kumar Gupta received the M. Tech. degree in Communication Engineering from Indian Institute of Technology, Mumbai, India in 2002. From February 2002 to September 2005, he worked as lecturer in the department of Electronics and Communication Engineering of Kumaon Engineering College, Dwarahat, Uttarakhand, INDIA. Later he joined the department of Electronics and Communication Engineering of National Institute of Technology (NIT), Silchar, India as lecturer in

September 2005 and is currently there at the post of Assistant Professor. His research area includes modeling and simulation of novel device structures on SOI MOSFETs. He is a member of IEEE Electron Device and Solid State Circuits Societies.

Srimanta Baishya received his B.E. in Electrical Engineering from Assam Engineering College, Assam, India; M.Tech. in Electrical Engineering from IIT Kanpur, India and Ph.D. in Electronics and Telecommunication Engineering from Jadavpur University, Kolkata, India. Dr. Baishya is currently working as a Professor, ECE Department, NIT Silchar, India. He has more than 25 publications in

National/International Journals/Conferences. His present research interest includes MOS Transistor Modeling, Semiconductor Devices Physics, VLSI circuits, and MEMS. He is a member of IEEE.