A 5-Level Three-Phase Cascaded Hybrid Multilevel Inverter

P. Thongprasri

Abstract—**This paper presents a 5-level three-phase cascaded hybrid multilevel inverter that consists of a standard 3-leg (one leg for each phase) and H-bridge in series with each inverter leg with separate DC voltage sources, 24V and 48V. The control signals for this hybrid multilevel inverter are implemented by a FPGA controller using PWM signal modulated technique and digital technique. A 5-level three-phase cascaded hybrid multilevel inverter model based on PSCAD/EMTDC is presented in this paper. The proposed hybrid multilevel inverter is described in detail that it is verified experimentally in three types of load; 18W fluorescent lamp-ballast, RL, and 1HP 3-phase induction motor; without filtering. Results of the experiment; the output waveform of line-line and phase voltages has 5 levels that percent of THD is between 15.6% and 18.3%, the output waveform of phase current is close to sinusoidal that percent of THD is between 2.7% and 4.2%.**

Index Terms—**Hybrid multilevel inverter, PSCAD/EMTDC, FPGA controller, h-bridge.**

I. Introduction

A multilevel inverter is a power electronic converter built to synthesize a desired AC voltage from several levels of DC voltages which the DC levels were considered to be identical in that all of them were batteries, solar cells, capacitors, etc. The multilevel inverter has gained much attention in recent years due to its advantages in lower switching loss better electromagnetic compatibility, higher voltage capability, and lower harmonics [1]-[3]. Several topologies for multilevel inverters have been proposed; the most popular being the diode-clamped [4], [5], flying capacitor [6], and cascade H-bridge [7] structures. Besides the three basic multilevel inverter topologies; other multilevel converter topologies have been proposed, most of these are hybrid circuits that are combinations of two of the basic multilevel topologies. The schemes of multilevel inverters are classified in to two types the multicarrier sub-harmonic pulse width modulation (MC-SH PWM) and the multicarrier switching frequency optimal pulse width modulation (MC-SFO PWM) [8], [9]. The MC-SH PWM cascaded multilevel inverter strategy reduced total harmonic distortion and the MC-SFO PWM cascade multilevel inverter strategy enhances the fundamental output voltage [10].

The THD will be decreased by increasing the number of levels. It is obvious that an output voltage with low THD is desirable, but increasing the number of levels needs more hardware, also the control will be more complicated. It is a tradeoff between price, weight, complexity and a very good output voltage with lower THD. Fig. 1 shows single phase topology of the diode Clamped, flying capacitor, a cascaded H-bridge, and cascade hybrid multilevel inverter that they have the number of switches, diodes, and capacitors as shown in table I (a 5- level multilevel inverter).

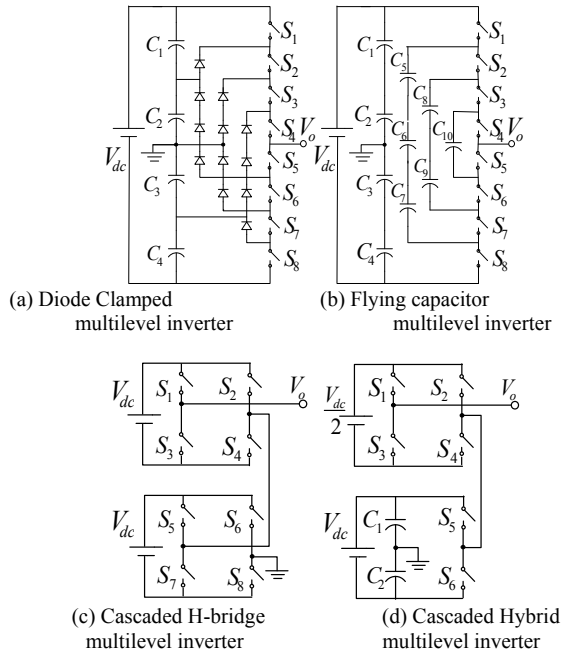

Fig. 1. One phase of a 5-level multilevel inverter.

TABLE I: Components of One Phase of A-5 Level Multilevel Inverter

Types of multilevel inverter	Number of switches	Number of diodes	Number of capacitors
Diode Clamped	8	12	4
Flying capacitor	8	-	10
Cascaded H-bridge	8	-	-
Cascade hybrid	6	-	2

In this paper, the proposed a 5-level three-phase cascaded hybrid multilevel inverter includes a standard 3-leg inverter (one leg for each phase) and H-bridge in series with each inverter leg as shown in Fig. 2. To develop the model of a 5-level cascaded hybrid multilevel inverter, a simulation is done based on PSCAD/EMTDC. All signals for controlling the hybrid multilevel inverter are created by a FPGA controller using PWM signal modulated technique and digital technique. The prototype is tested with 3 types of load; a 18W fluorescent lamp-ballast, RL (R is $265\,\Omega$, L is $0.125\,H$), and a 1HP 3-phase induction motor (no load); without filtering.

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P. Thongprasri is with the Department of Electrical Engineering, Faculty of Engineering at Si Racha, Kasetsart University Si Racha Campus, Chonburi, Thailand (e-mail: sfengprt@ src.ku.ac.th).

II. Operation Principle of the Hybrid Multilevel Inverter

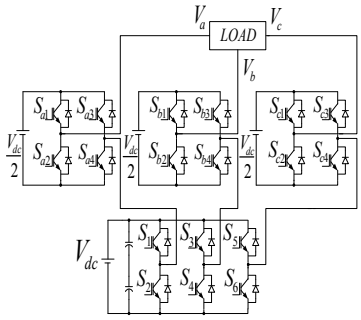

Fig. 2. Topology of a 5-level three-phase cascaded hybrid multilevel inverter.

Fig. 2 shows the topology of the proposed a 5-level 3-phase cascaded hybrid multilevel inverter. Single phase topology of the hybrid multilevel inverter is shown in Fig. 3; the bottom is one leg of a standard 3-leg inverter with a dc power source (V_{dc}), the top is a hybrid in series with each standard inverter leg that the H-bridge inverter can use a separate dc power source ($V_{dc}/2$). Considering the output voltage v_1 of this leg is either $+V_{dc}/2$ when S_1 closed or $-V_{dc}/2$ when S_2 closed. This leg is connected in series with a full H-bridge inverter, then the output voltage v_2 of the H-bridge inverter is either $+V_{dc}/2$ when S_{a1}, S_{a4} closed, 0 when S_{a1}, S_{a3} or S_{a2}, S_{a4} closed, or $-V_{dc}/2$ when S_{a2}, S_{a3} closed. An example output waveform that this topology can achieve as shown in the Fig. 4, when the output voltage $v = v_1 + v_2$ is required to be zero, one can either set $v_1 = +v_{dc}/2$ and $v_2 = -v_{dc}/2$ or $v_1 = -v_{dc}/2$, and $v_2 = +v_{dc}/2$.

In [11], several different two-level multilevel carrier-based PWM techniques have been extend for controlling the active devices in a multilevel converter, the most popular and easiest technique to implement uses several triangle carrier signals and one reference, or modulation, signal per phase. In order to achieve better dc link utilization at high modulation indices, the sinusoidal reference signal can be injected by a third harmonic with a magnitude equal to 25% of fundamental.

Fig. 5 shows MC-SH PWM of a 5-level inverter, m-1 carriers with the same frequency f_c and the same amplitude A_c are dispose such that the bands they occupy are contiguous, The reference waveform has peak-to-peak amplitude A_m, a frequency f_m, and its zero centered in the middle of the carrier set, The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device corresponding to that carrier is switched on, and if the reference is less than a carrier signal, then the active device corresponding to that carrier is switched off.

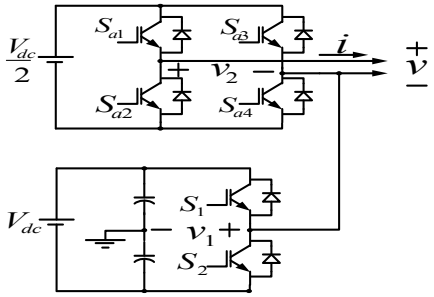

Fig. 3. Single phase topology of the hybrid multilevel inverter.

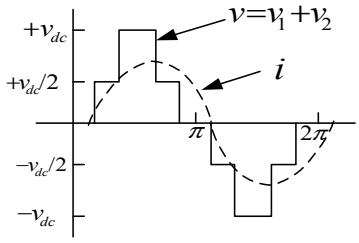

Fig. 4. Output waveform of the hybrid multilevel inverter.

Fig. 6 shows the relationship between the sinusoidal reference signal and the triangular signal which used to create the PWM signal; the output of the PWM signal is either 1, when $V_{ctrl} > V_{tri}$ or 0 when, $V_{ctrl} < V_{tri}$, and the PWM signal width can be written as equation (1).

$$T_{PWM} = A_{ctrl} \cdot T_{tri} \quad ;0 \le A_{ctrl} \le 1 \tag{1}$$

Nomenclature:

T_{PWM} Width of the PWM signal.

A_{ctrl} Height of the control signal.

T_{tri} Period of the triangular signal.

V_{ctrl} Output voltage of the control signal.

V_{tri} Output voltage of the triangular signal.

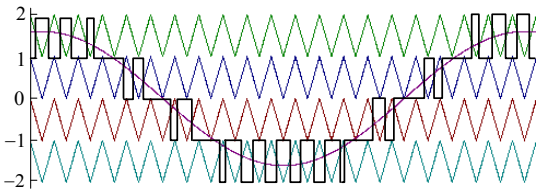

Fig. 5. MC-SH PWM of a 5-level inverter.

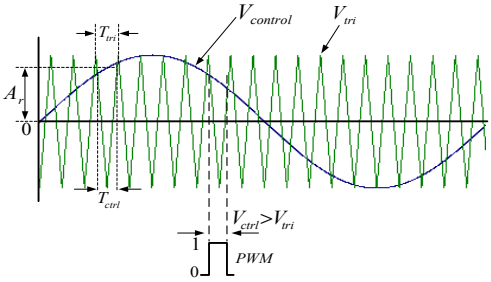

Fig. 6. The relationship between the sinusoidal referencesignal and the triangular signal.

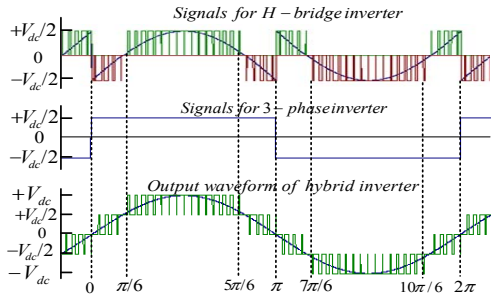

Fig. 7. Output waveform of the 5-level hybrid multilevel inverter.

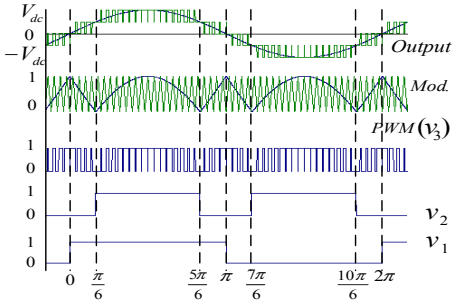

Fig. 8. Signals for controlling the hybrid multilevel inverter.

Fig. 7 shows output waveform of the 5-level cascaded hybrid multilevel inverter that it is used to be the pattern to create the control signal for hybrid multilevel inverter. PWM (v_3), v_1, and v_2 signals shown in Fig. 8 are the parameters in digital process to create all control signals that they are shown in table II. Modulated signal is created as equation (2) and (3), amplitude modulation index m_a can be found at the following equation (4); m_a in this paper is 0.8.

$$T_{PWM} = m_a T_{tri}(1-2\sin(\omega t)) \quad ;\begin{cases} 0 \le \omega t < \dfrac{\pi}{6} \\ \dfrac{5\pi}{6} < \omega t \le \pi \end{cases} \tag{2}$$

$$T_{PWM} = m_a T_{tri}(2\sin(\omega t)-1) \quad ; \frac{\pi}{6} \le \omega t \le \frac{5\pi}{6} \tag{3}$$

$$m_a = \frac{V_{ctrl}}{V_{tri}} \tag{4}$$

TABLE II: DIGITAL PROCESS OF THE CONTROL SIGNALS.

Electronic switch devices	Digital process
s_1	v_1
s_2	$\overline{v_1}$
s_{a1}	$v_3 \cdot ((v_1 \cdot v_2) + (\overline{v_1} \cdot \overline{v_2}))$
s_{a2}	$\overline{v_3} \cdot \overline{((v_1 \cdot v_2) + (\overline{v_1} \cdot \overline{v_2}))}$
s_{a3}	$v_3 \cdot \overline{((v_1 \cdot v_2) + (\overline{v_1} \cdot \overline{v_2}))}$
s_{a4}	$\overline{v_3} \cdot ((v_1 \cdot v_2) + (\overline{v_1} \cdot \overline{v_2}))$

III. SIMULATION RESULTS

The simulation model based on PSCAD/EMTDC is shown in appendix; V_{dc} are 24V and 48V, RL load (R is 265 Ω , L is 0.125 H), sinusoidal reference signal frequency is 50Hz, carrier signal frequency is 2,500Hz, and m_a is 0.8.

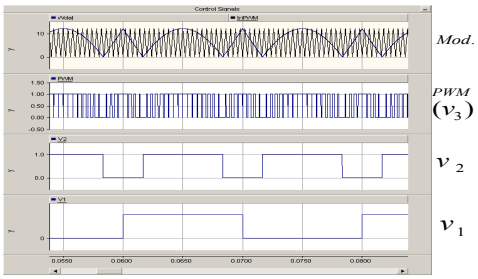

Fig. 9. Simulation result of v_1, v_2, v_3, and modulated signal.

Results of the simulation; Fig. 9 shows modulated signal, v_1, v_2, and PWM (v_3) signals. Fig. 10 shows all control signals for the power electronic switches. Fig. 11 shows the output waveform of phase voltage and phase current.

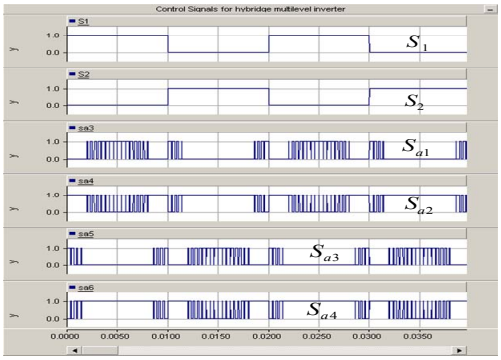

Fig. 10. Simulation result of all control signals for electronic switch devices (IGBTs).

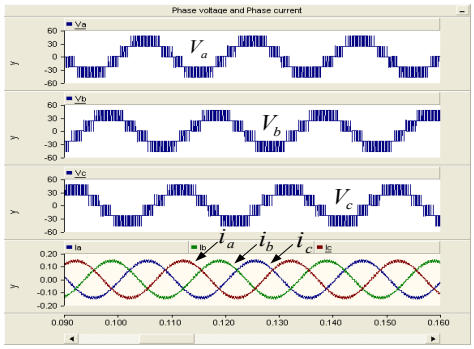

Fig. 11. Simulation result of phase voltage and phase current when load is RL (R is 265 Ω , L is 0.125 H).

IV. EXPERIMENTAL RESULTS

Fig. 12 shows the topology of the hybrid multilevel inverter with separate DC voltage sources ;24V and 48V; that the IGBTs (GT60M303) are used to be power electronic switches in the H-bridge inverter, and the IGBT modules (CM75DU-12H) are used to be power electronic switches in the 3-phase inverter. The output voltage of the hybrid

multilevel inverter is connected to a 3-phase step up transformer (55/380V/50Hz, Y-Y) rated 1.5kW. Prototype of the 1kW 5-level three-phase cascaded hybrid multilevel inverter as shown in Fig. 13 has been built in order to verify the proposed hybrid multilevel inverter. The control signals in this paper are created by the field programmable gate array (FPGA, discovery–III XC3S200 model) controller. Fig. 14 shows three signals; PWM (v_3), v_1, and v_2; for the hybrid multilevel inverter, modulation index is 0.8.

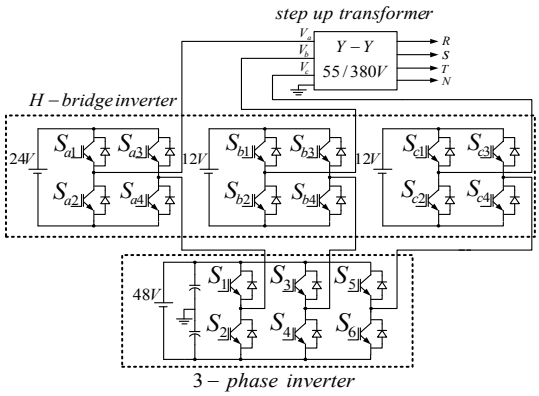

Fig. 12. Topology of the hybrid multilevel inverter with separate DC voltage sources; 24V and 48V.

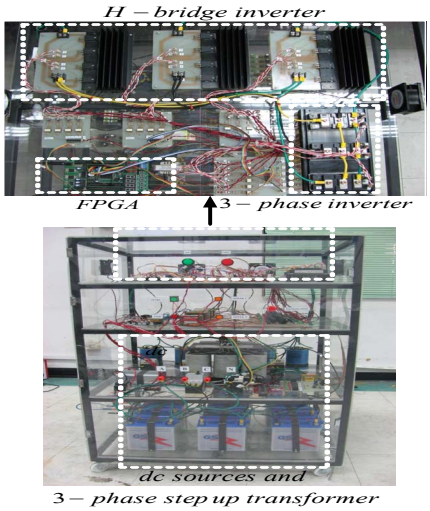

Fig. 13. Prototype of the 5-level 3-phase cascaded hybrid multilevel inverter.

Fig. 15 shows prototype of the 1kW 5-level three-phase cascaded hybrid multilevel inverter with a 18W fluorescent lamp-ballast load. Fig. 16 shows the experimental results including phase voltage and phase current; the output phase voltage waveform has 5 levels that its *rms* voltage is 225V, and the phase current waveform is close to sinusoidal that its *rms* current is 360mA. Fig. 17 shows the experimental result including output waveform of line-line voltage and line-line that voltage THD is 17.4%, 16.6%, and 18%.

Fig. 18 shows prototype of the 1kW 5-level three-phase cascaded hybrid multilevel inverter with RL load (R is 265 Ω, L is 0.125 H). Fig. 19 shows the experimental results including phase voltage and phase current; the output phase voltage waveform has 5 levels that its *rms* voltage is 195V, and the phase current waveform is close to sinusoidal that its *rms* current is 708mA. Fig. 20 shows the experimental result including the phase voltage THD of 17% and phase current THD of 2.7%. Fig. 21 shows the experimental result including output waveform of line-line voltage that line-line voltage THD is 17.9%, 17.4%, and 18.3%.

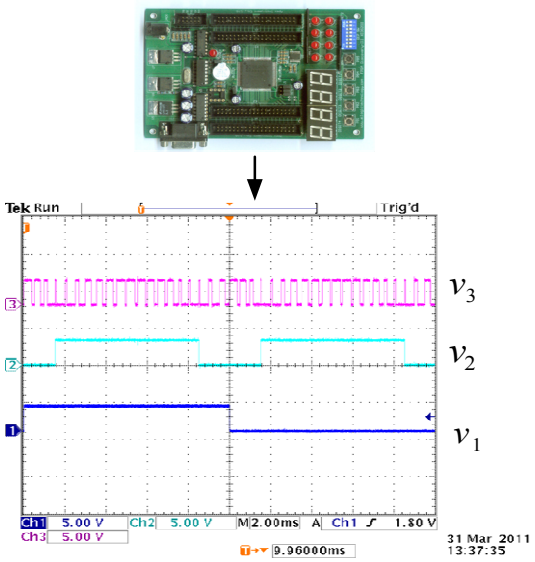

Fig. 14. The control signals for hybrid multilevel inverter are created by FPGA (m_a =0.8).

Fig. 15. Prototype of the 1kW 5-level three-phase cascaded hybrid multilevel inverter with 3 fluorescent lamp-ballast loads.

Fig. 22 shows prototype of the 1kW 5-level three-phase cascaded hybrid multilevel inverter with a 3-phase induction motor load (no load). Fig. 23 shows the experimental results including phase voltage and phase current; the output phase voltage waveform has 5 levels that its *rms* voltage is 206V, and the phase current waveform is close to sinusoidal that its *rms* current is 786mA, and the output frequency is 50Hz. Fig. 24 shows the experimental result including the phase voltage THD of 16%, and phase current THD of 4.2%. Fig. 25 shows the experimental result including output waveform of line-line voltage that line-line voltage THD is 16.2%, 15.6%, 16.7%, and the output frequency is 50 Hz.

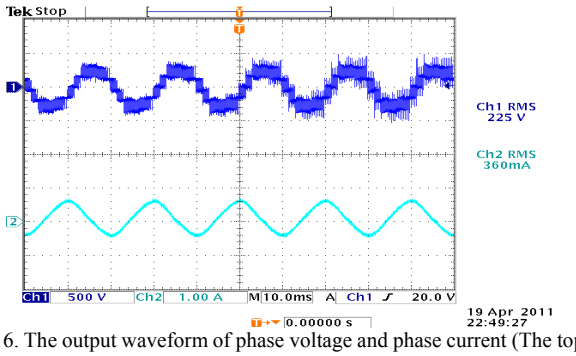

Fig. 16. The output waveform of phase voltage and phase current (The top is phase voltage that its *rms* voltage is 225V, the bottom is phase current that its *rms* current is 360mA).

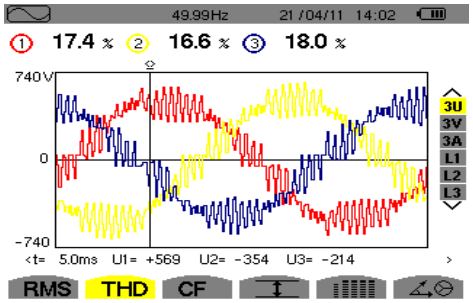

Fig. 17. The output waveform of line-line voltage that line-line voltage THD is 17.4%, 16.6%, and 18%. The output frequency is 50Hz.

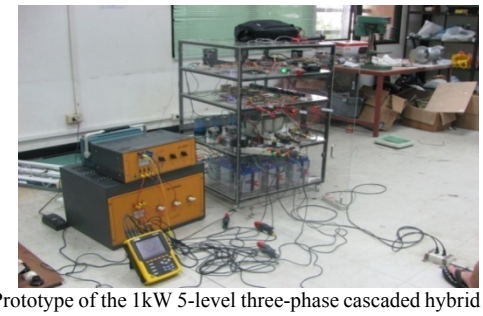

Fig. 18. Prototype of the 1kW 5-level three-phase cascaded hybrid multilevel inverter with RL load (R is 265 Ω , L is 0.125 H).

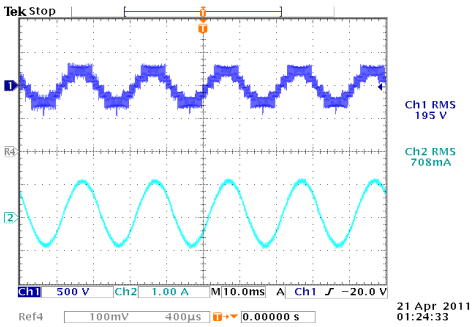

Fig. 19. The output waveform of phase voltage and phase current (The top is phase voltage that its *rms* voltage is 195V, the bottom is phase current that its *rms* current is 708mA).

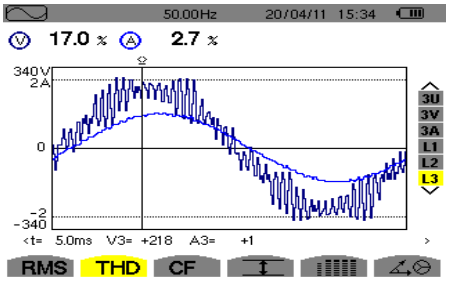

Fig. 20. Phase voltage THD of 17%, phase current THD of 2.7%, the output frequency is 50 Hz. (RL load, R is 265 Ω , L is 0.125 H).

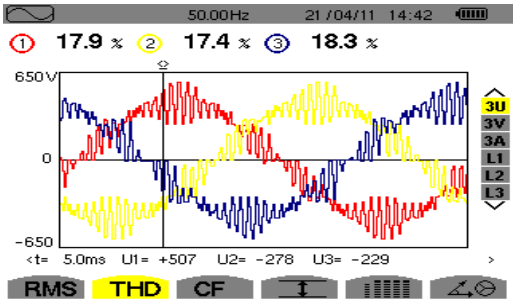

Fig. 21. The output waveform of line-line voltage that line-line voltage THD is 17.9%, 17.4%, and 18.3%. The output frequency is 50Hz.

Fig. 22. Prototype of the 1kW 5-level three-phase cascaded hybrid multilevel inverter with a 3-phase induction motor rated 1HP load (no load).

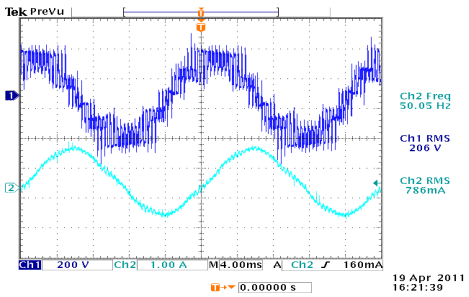

Fig. 23 . The output waveform of phase voltage and phase current (The top is phase voltage that its *rms* voltage is 206V, the bottom is phase current that its *rms* current is 786mA).

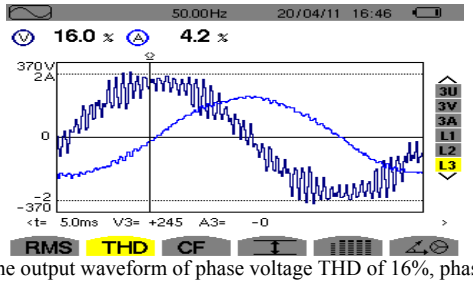

Fig. 24. The output waveform of phase voltage THD of 16%, phase current THD of 4.2%. The output frequency is 50 Hz.

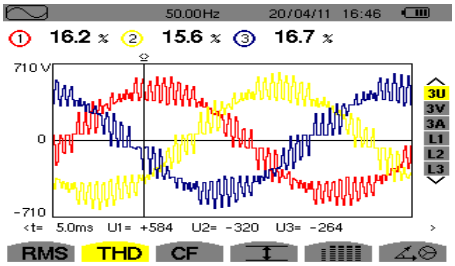

Fig. 25. The output waveform of line-line voltage that line-line voltage THD is 16.2%, 15.6%, 16.7%. The output frequency is 50Hz.

V. Conclusion

Prototype of the 5-level three-phase cascaded hybrid multilevel inverter consists of a 3-phase inverter and 3 H-bridge inverters that it uses separate dc power sources; 24V and 48V. The control signals for power electronic switches are created by FPGA controller using PWM signal modulated technique and digital technique. The prototype is tested with three types of load; 18W fluorescent ballast-lamp, RL, and 3-phase induction motor rated 1HP; without filtering. Results of the test; the output line-line and phase voltages has 5 levels that its THD voltage is between 15.6% and 18.3%, the output waveform of phase current is close to sinusoidal that its THD current is between 2.7% and 4.2%.

APPENDIX

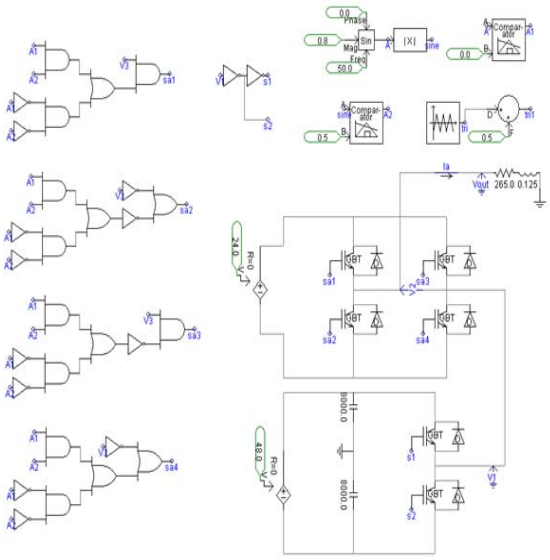

Fig. 26. The simulation model of a 5-level three- phase cascaded multilevel inverter based on pscad/emtdc (single phase).

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P. Thongprasri was born in Suphanburi, Thailand, on June 19, 1971. He received the B.Eng. degree in electronic engineering and M.Eng. degree in electrical Engineering from King Mongkut Institute of Technology Ladkrabang, Thailand, in 1995 and 2005, respectively. He is currently lecturer at the Department of Electrical Engineering, Faculty of Engineering at Si Racha, Kasetsart University Si Racha Campus, Thailand. His research interests are Power Converters, Power Electronics, Robotics, Applications of Microcontroller and FPGA controller.