

New Electronically Tunable Voltage-Mode Lowpass, Highpass, Bandpass Filter Using Simple OTAs

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Abstract—This paper presents a new electronically tunable voltage-mode universal biquad filter based on simple CMOS operational transconductance amplifiers (OTAs) and grounded capacitors. The proposed filter provides second-order lowpass, bandpass and highpass voltage responses at a high impedance input terminal, which enable easy cascading. The circuit enjoys realization using a low number of active and passive components, no requirement with the component choice conditions to realize all filtering functions, and low active and passive sensitivities performance. The performances of the proposed filter are simulated with PSPICE to confirm the presented configuration.

Index Terms—voltage-mode filter, electronically tunable, operational transconductance amplifier, CMOS

I. INTRODUCTION

Operational transconductance amplifiers (OTAs) have exhibited some advantages in the circuit design, because its transconductance gain can be varied electronically which is especially suitable for analog circuits. The OTA provides a wide tunable range and powerful ability to generate various circuits. Moreover, OTA based circuits require no resistors and, therefore, are suitable for integrated circuit (IC) implementation [1].

A biquad filter is very useful block to realize high-order filters that plays an important role in the fields of electronic measurement, communication, automatic control and neural networks. Besides, the voltage-mode active filters with high input impedance are of great interest because several cells of this kind can be directly connected in cascade to implement higher order filters [2]. On the other hand, the filters using grounded capacitors are beneficial from the point of view of IC implementation [3]. In the literature, several voltage-mode biquad filters using OTAs have been proposed [4]-[23]. Considering the number of input and output ports, these filters can be divided into four categories: (i) a single-input, single-output (SISO) type [4]-[6], (ii) a single-input, multiple-output (SIMO) type [1], [7]-[12], (iii) a multiple-input, single-output (MISO) type [13]-[16], and (iv) a multiple-input, multiple-output (MIMO) type [17]-[23]. Generally, the SISO filters can realize multi-function outputs by altering the connection way of the circuits [4]-[6], but altering the connection way can only realize a filtering output at a time. The MISO and MIMO filters can realize multifunction outputs simultaneously [13]-[23], but they

need input signal matching. The SIMO filters can simultaneously realize standard filters, namely lowpass (LP), bandpass (BP) and highpass (HP) filters at a time without altering the connection way of the circuits and without input signal matching. This property is interested in this paper.

In the proposed voltage-mode OTA-based SIMO filtering circuits, circuit [1] contains four OTAs and enjoys low active and passive sensitivities, but the filter structure requires capacitor injection of excitation signals in the circuit design, so it is not suitable for cascade implementation, and the resulting floating capacitor are not ideal for IC implementation. The circuits [7], [8], [11], [12] use grounded capacitors and enjoy a high impedance input terminal, but they suffer from the use of large active components. The circuits [9], [10] can realize standard filtering, but the circuits require component-matching condition for realizing all filter responses and also use two kinds of active components (OTA and op-amp [9] and OTA and DDCC [10]).

In this paper, a new electronically tunable voltage-mode universal biquad filter employing simple CMOS OTAs and grounded capacitors, which provides the advantage of electronic tuning capability and is especially interest from the IC implementation point of view, is proposed. It involves only a kind of active component. The circuit can realize LP, BP and HP voltage responses at a high input impedance terminal, which enable easy cascading. Also, the natural frequency (ω_o) and the quality factor (Q) can be set orthogonally by adjusting the circuit components. In addition, the bandstop (BS) and allpass (AP) responses can be obtained by interconnection of relevant output voltages by using additional circuits. PSPICE simulation results are used to verify the performances of the proposed circuit.

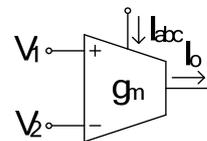


Fig. 1. Circuit symbol of the OTA.

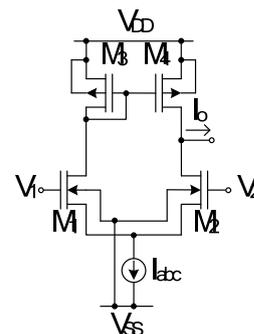


Fig. 2. The CMOS implementation of the simple OTA.

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II. CIRCUIT DESCRIPTION

The circuit symbol of the OTA is shown in Fig. 1. It is assumed an ideal voltage-controlled current source that has infinite input and output impedances. Its characteristic of ideal OTA can be given by

$$I_o = g_m(V_1 - V_2) \tag{1}$$

where I_o is the output current, g_m is the transconductance gain, and V_1 and V_2 denote non-inverting and inverting input voltage, respectively. Fig. 2 shows the CMOS implementation of the simple OTA. It uses only four MOS transistors and one current source. Assuming four transistors are operated in saturation region, the transconductance gain g_m of this OTA can be calculated as

$$g_m = \sqrt{\mu C_{ox} (W/L) I_{abc}} \tag{2}$$

where I_{abc} is the bias current, μ is the carrier mobility, C_{ox} is the gate oxide capacitance per unit area, and W and L are the channel width and length, respectively.

Based on the use of simple CMOS OTA, the addition/subtraction voltage signal can be shown in Fig. 3. Referring to [24], [25], this circuit may be called a ‘pool circuit’. Assume that all the NMOS devices are biased in the saturation region with individual wells connected to their sources to eliminate the body effect, let the transconductance parameter and the threshold voltage of M_1 through M_4 be equal to K and V_{TH} , respectively, $I_{abc1}=I_{abc}$ and $I_{abc2}=I_{abc}$ are two current sources, the currents I_{o1} and I_{o2} can be given as [24], [25]

$$I_{o1} = K(V_1 - V_o) \sqrt{\frac{2I_{abc}}{K} - (V_1 - V_o)^2} \tag{3}$$

$$I_{o2} = K(V_3 - V_2) \sqrt{\frac{2I_{abc}}{K} - (V_3 - V_2)^2} \tag{4}$$

at the equilibrium state [24], [25]

$$V_o = V_1 - V_2 + V_3. \tag{5}$$

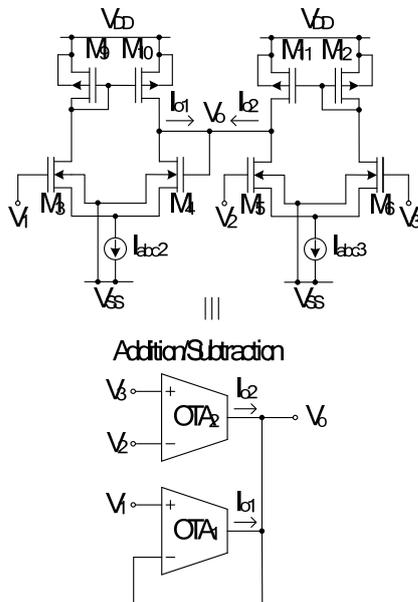


Fig. 3. The addition/subtraction circuit using simple OTAs.

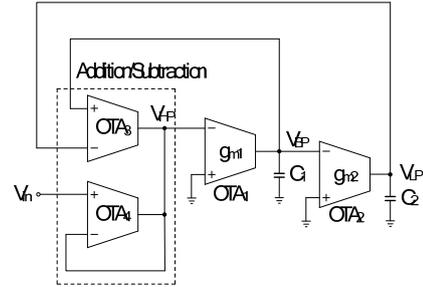


Fig. 4. Proposed voltage-mode biquad filter using OTAs.

This circuit operates as a pool [24], [25] in the sense that the currents flowing in and flowing out are in equilibrium at the output node V_o . Therefore, the addition and subtraction operation for voltage signals can be performed by the circuit in Fig. 3.

The proposed voltage-mode universal biquad filter is shown in Fig. 4. The buffer circuits must be added at the output terminals of Fig. 4, because the output impedances of this circuit are not zero. By routine circuit analysis, the voltage transfer function of Fig. 4 can be given by

$$\frac{V_{HP}}{V_{in}} = \frac{s^2 C_1 C_2}{s^2 C_1 C_2 + s C_2 g_{m1} + g_{m1} g_{m2}} \tag{6}$$

$$\frac{V_{BP}}{V_{in}} = \frac{-s C_2 g_{m1}}{s^2 C_1 C_2 + s C_2 g_{m1} + g_{m1} g_{m2}} \tag{7}$$

$$\frac{V_{LP}}{V_{in}} = \frac{g_{m1} g_{m2}}{s^2 C_1 C_2 + s C_2 g_{m1} + g_{m1} g_{m2}} \tag{8}$$

Thus, the proposed circuit can realize a non-inverting HP signal at V_{HP} , an inverting BP signal at V_{BP} and a non-inverting LP signal at V_{LP} without requirement critical component matching conditions. In this case, the circuit employs only 16 MOS transistors and 4 current sources (four simple OTAs) and two grounded capacitors. Then, the filter structure is a particularly attractive for IC implementation because there is no resistor requirement and using only grounded capacitor.

The natural frequency (ω_o) and the quality factor (Q) can be given as

$$\omega_o = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}} \tag{9} \quad Q = \sqrt{\frac{g_{m2} C_1}{g_{m1} C_2}} \tag{10}$$

Letting $g_m = g_{m1} = g_{m2}$, the parameters ω_o and Q can be rewritten as

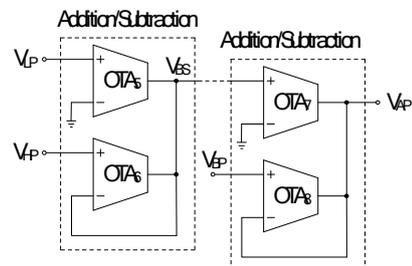


Fig. 5. Adder voltage using OTAs.

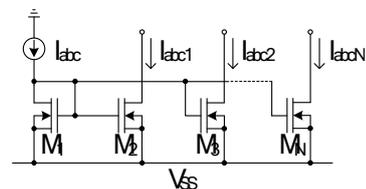


Fig. 6. Multiple-output current source.

$$\omega_o = g_m \sqrt{\frac{1}{C_1 C_2}} \quad (11)$$

$$Q = \sqrt{\frac{C_1}{C_2}} \quad (12)$$

From above equations, the parameter Q can be set by C_1 and C_2 whereas the parameter ω_o can be tuned by adjusting the transconductance g_m through the bias currents/voltages of the OTAs without disturbing Q , hence the name “electronically tunable filter”.

In addition, by adding non-inverting LP and non-inverting HP filter responses, a BS filter response can be easily obtained ($V_{BS}=V_{LP}+V_{HP}$). Similarly, an AP filter response can be obtained by adding with non-inverting LP, inverting BP and non-inverting HP filter responses ($V_{AP}=V_{LP}+V_{BP}+V_{HP}$). Typically, voltage-mode addition circuit can be realized by using operational amplifiers and attached to resistors. However, the author provides the adder circuit in Fig. 5 for suitable IC implementation as one choice. The adder circuit of Fig. 5 is composed of four simple CMOS OTAs, as above already mentioned. By using the circuit in Fig. 5, the BS and AP voltage responses can be obtained as

$$\frac{V_{BS}}{V_{in}} = \frac{s^2 C_1 C_2 + g_{m1} g_{m2}}{s^2 C_1 C_2 + s C_2 g_{m1} + g_{m1} g_{m2}} \quad (13)$$

$$\frac{V_{AP}}{V_{in}} = \frac{s^2 C_1 C_2 - s C_2 g_{m1} + g_{m1} g_{m2}}{s^2 C_1 C_2 + s C_2 g_{m1} + g_{m1} g_{m2}} \quad (14)$$

Therefore, the proposed voltage-mode universal biquad filter can realize five standard filtering functions by using only eight simple CMOS OTAs (32 MOS transistors and 8 current sources). Moreover, the input V_{in} is connected to the high impedance input nodes of the OTA. So, the circuit enjoys the advantage of having high input impedance.

Note from the proposed filter that it requires no component-matching condition for realization all filter responses. In fact, the addition/subtraction circuit is requires current-matching condition (i.e. $I_{abc3}=I_{abc4}$), but this problem can be easily solved by using multiple-output current source. However, the author provides the simple multiple-output current source in Fig. 6 as one example. If more accuracy current mirror is required, cascode current mirror or Wilson current mirror may be used to replace the simple current mirror in Fig. 6.

III. CIRCUIT ANALYSIS

Taking the non-idealities of the addition/subtraction circuit, the equation (5) can be rewritten as

$$V_o = \beta_1 V_1 - \beta_2 V_2 + \beta_3 V_3 \quad (15)$$

where $\beta_1(s)=\beta_1=1-\varepsilon_{1v}$ and $\varepsilon_{1v}(|\varepsilon_{1v}| \ll 1)$ denotes the voltage tracking error from V_1 terminal to V_o terminal of the k -th addition/subtraction circuit, $\beta_2(s)=\beta_2=1-\varepsilon_{2v}$ and $\varepsilon_{2v}(|\varepsilon_{2v}| \ll 1)$ denotes the voltage tracking error from V_2 terminal to V_o terminal of the k -th addition/subtraction circuit, $\beta_3(s)=\beta_3=1-\varepsilon_{3v}$ and $\varepsilon_{3v}(|\varepsilon_{3v}| \ll 1)$ denotes the voltage tracking

error from V_3 terminal to V_o terminal of the k -th addition/subtraction circuit.

Considering the non-idealities of the OTA, the transconductance gain g_{mni} can be given that

$$g_{mni} = \frac{g_{mi} \omega_{gi}}{s + \omega_{gi}} \quad (i=1,2) \quad (16)$$

where ω_{gi} denotes the first-order high frequency pole of the OTA_{*i*} ($i=1,2$). Referring to [22], the transconductance gain g_{mni} can be modified as

$$g_{mni} = g_{mi} (1 - \mu_i s) \quad (17)$$

where $\mu_i=1/\omega_{gi}$. Using (15) and (17), the denominator of the non-ideal biquad can be expressed as

$$D(s) = s^2 (C_1 C_2 - C_1 g_{m2} \mu_1 \beta_1 + g_{m1} g_{m2} \mu_1 \mu_2 \beta_2) + s g_{m2} (C_1 \beta_1 - g_{m1} \mu_2 \beta_2 - g_{m1} \mu_1 \beta_2) + g_{m1} g_{m2} \beta_2 \quad (18)$$

The non-ideal natural frequency (ω_{on}) and the non-ideal quality factor (Q_n) can be obtained as

$$\omega_{on} = \sqrt{\frac{g_{m1} g_{m2} \beta_2}{C_1 C_2 \left(1 - \frac{C_1 g_{m2} \mu_1 \beta_1 + g_{m1} g_{m2} \mu_1 \mu_2 \beta_2}{C_1 C_2} \right)}} \quad (19)$$

$$Q_n = \frac{\sqrt{C_1 C_2 g_{m1} g_{m2} \beta_2 \left(1 - \frac{C_1 g_{m2} \mu_1 \beta_1 + g_{m1} g_{m2} \mu_1 \mu_2 \beta_2}{C_1 C_2} \right)}}{C_1 g_{m2} \beta_1 \left(1 - \frac{g_{m1} \mu_2 \beta_2 - g_{m1} \mu_1 \beta_2}{C_1 g_{m2} \beta_1} \right)} \quad (20)$$

However, due to the parasitic effects, the characteristics depart from the ideal response. But the parasitic effects can be made negligible by satisfying the following conditions:

$$\left. \begin{aligned} \frac{C_1 g_{m2} \mu_1 \beta_1 + g_{m1} g_{m2} \mu_1 \mu_2 \beta_2}{C_1 C_2} \ll 1 \\ \frac{g_{m1} \mu_2 \beta_2 - g_{m1} \mu_1 \beta_2}{C_1 g_{m2} \beta_1} \ll 1 \end{aligned} \right\} \quad (21)$$

IV. SIMULATION RESULTS

The performances of the proposed filter in Fig. 4 have been verified using PSPICE simulations. The simple OTA and addition/subtraction circuit in Figs. 2 and 3 were performed with 0.5 μ m CMOS technology provided by MOSIS. The aspect ratios of the transistors used are $W/L=2\mu\text{m}/2\mu\text{m}$ for the NMOS devices and $W/L=40\mu\text{m}/2\mu\text{m}$ for the PMOS devices. The bias currents are I_{abc3} through $I_{abc8}=25\mu\text{A}$ and the supply voltages are $\pm 3\text{V}$ [26].

For example design, $C_1=C_2=100\text{pF}$ and $I_{abc1}=I_{abc2}=50\mu\text{A}$ ($g_m=77.52\mu\text{S}$) are given. This setting has been designed to obtain the filter responses with the natural frequency of $f_o \cong 123.37\text{kHz}$ and the quality factor (Q)=1. The simulated response of the HP, BP, and LP of the proposed filter are shown in Fig. 7. In this figure, the pole frequency of 122.84kHz is obtained. The pole frequency is 122.84kHz instead of 123.37kHz owing to the effect described in Section

III. According to equation (19), this drop-off would be caused by voltage tracking errors. Fig. 8 shows the simulated a BP filter response of the proposed filter when the bias currents I_{abc} ($I_{abc}=I_{abc1}=I_{abc2}$) were simultaneously adjusted for the value 1, 10, 30 and $300\mu A$, respectively. This result is confirmed by (11).

By using adder circuit in Fig. 5, the simulation results for the BS ($V_{LP}+V_{HP}$) and AP ($V_{LP}+V_{BP}+V_{HP}$) voltage responses are shown in Figs. 9 and 10, respectively. It is evident from Figs. 7, 9 and 10 that HP, BP, LP, BS and AP voltage responses can be achieved by using eight simple CMOS OTAs and two grounded capacitors.

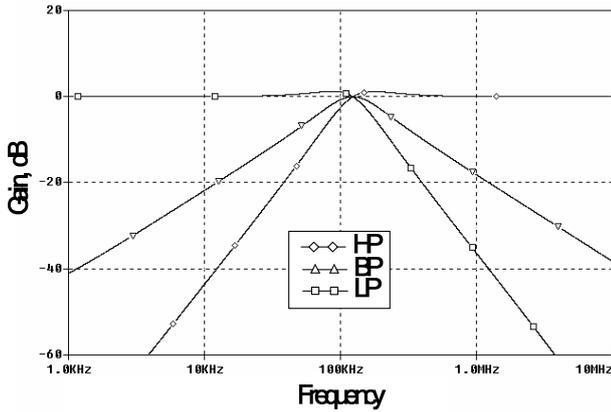


Fig. 7. Simulated frequency responses of the HP, BP and LP voltage responses of the proposed filter.

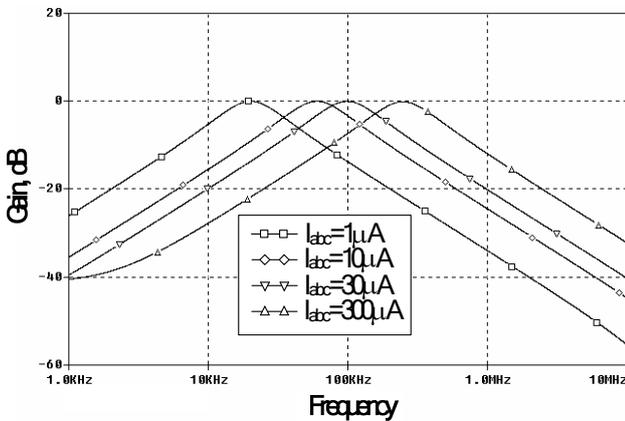


Fig. 8. Simulated frequency responses of the BP filter when I_{abc} is varied.

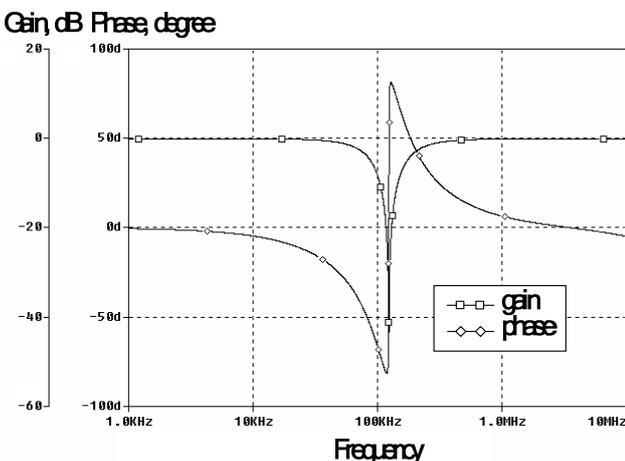


Fig. 9. Simulated frequency and phase responses of the BS filter.

A sine wave signal (122.84kHz) was supplied to the input of the BP response. When the amplitude is increased, it has been found that the input signal level is lower than $0.8V_{P-P}$ and the total harmonic distortion (THD) is about 0.7%. However, the THD is rapidly increased when the input signal is increased beyond $0.8V_{P-P}$. These simulation results are shown in Figs. 11 and 12, respectively.

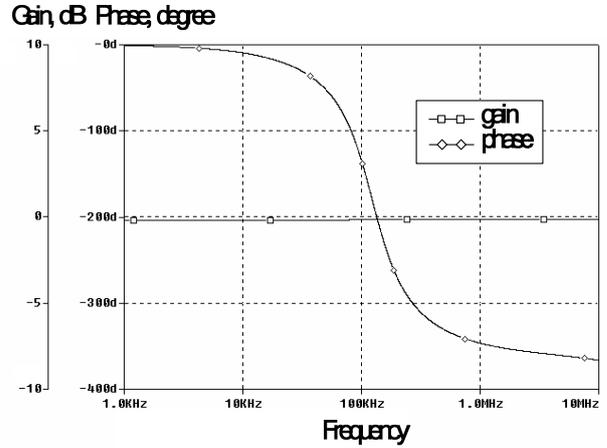


Fig. 10. Simulated frequency and phase responses of the AP filter.

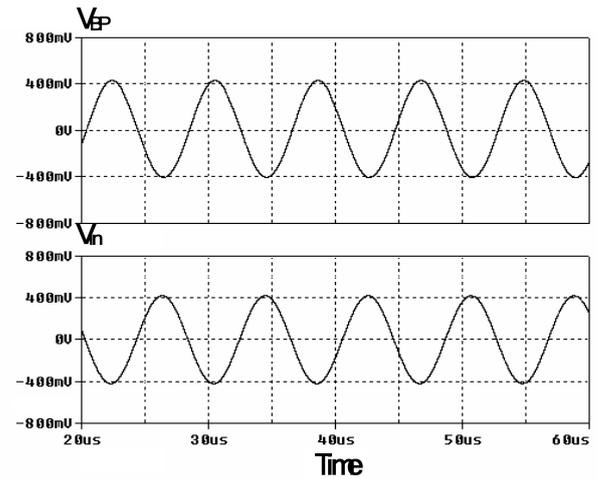


Fig. 11. The input and output waveforms of the BP responses for a 122.84kHz sinusoidal input voltage of $0.8V_{P-P}$.

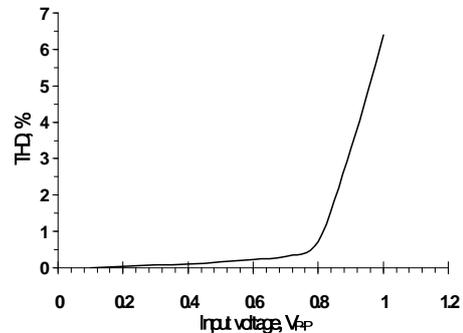


Fig. 12. Total harmonic distortion of BP filter on input voltage amplitude.

It should be noted that in order to confirm the operation of the proposed filter, this paper has been simulated by using capacitor value of 100pF. However, for on chip capacitor, the capacitance value should be ranged between 0.5 to 50pF [27],

[28]. If low value capacitance is used, the transconductance gain must be reduced for the proposed circuit to work within the bandwidth of the OTA.

V. CONCLUSION

In this paper, a new electronically tunable voltage-mode universal biquad filter based on simple CMOS OTAs and grounded capacitors, which is very suitable for IC implementation, is proposed. The proposed filter can realize LP, BP, HP, BS and AP filter responses. The ω_0 of the filter can electronically be controlled. Also, the Q can orthogonally be set by controlling the circuit components. The circuit requires no component matching conditions and no inverting-type voltage input signals and has low active and passive sensitivities. For realizing five standard filter responses, the filter employs only 32 MOS transistors and 8 current sources (8 simple CMOS OTAs).

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