Optimum Repeater Insertion for on-chip Global Interconnects in High Performance Deep Submicron ICs

P.V.Hunagund and A.B.Kalpana

Abstract—**This paper addresses the problem of power dissipation during buffer insertion phase of interconnect performance optimization. It is shown that the interconnect delay is actually very shallow with respect to both the repeater size and separation close to the minimum point. A methodology is developed to calculate the repeater size and interconnect length which minimizes the total interconnect power dissipation for any given delay penalty. This methodology is also used to quantify relative importance of various components of the power dissipation for power-optimal solutions for various technology nodes.**

Index Terms—**Buffer, Dynamic power, Interconnect, Short circuit power, Technology nodes**.

I. INTRODUCTION

The power dissipation in high performance integrated circuits (ICs) is quickly becoming a performance bottleneck. The scaling paradigm will exacerbate the power problem severely from many different angles. On one hand the device leakage power due to sub threshold and gate leakage is likely to rise in the future. On the other hand, the dynamic power will also increase not only due to a larger number of devices and interconnects on the chip, but also owing to the burden of keeping the speeds of electrical interconnects compatible with increasing clock frequencies. Certain estimates, which merely include device power (both dynamic and static), have shown chip power densities to increase to about 200 W/cm^2 at 35 nm node[1]. Including the interconnect power would substantially increase these power density estimates. This may lead to a significant increase in the chip temperature, which would degrade both reliability, through greater susceptibility to electro migration failures, and performances, through increased interconnect resistance and poorer device characteristics. The situation presents an impending power crisis, which threatens to slow down the progress of the chip industry.

It is important to identify the major power consumption sources on a chip, quantify them, and focus on efficient technological, circuit and/or architectural solutions to minimize them. Toward this goal, we address a potentially large source of chip power. the power required for global signaling. Various techniques has been proposed [2], [3], [4],[5] for power optimization of global signaling. Paper [6] presents a methodology to achieve the optimal wire sizing of buffered global interconnects, but it considers only RC effect. But for deep submicron IC's considering inductance effects also essential. We first deal with a realistic estimation of the power consumption in global wires including that due to repeaters, used to speed these wires. Having quantified this as a function of future technology nodes, we then introduce a efficient, methodology which minimizes the power consumed by repeaters in global interconnects.

For an RC line, repeater insertion outperforms wire sizing. It is shown in this paper that this behavior is not the case for an RLC line. The minimum signal propagation delay always decreases with increasing line width for RLC lines if an optimum repeater system is used. With increasing demand for low-power ICs, different strategies have been developed to minimize power in the repeater insertion process. The line inductance, however, has yet to be considered in the optimization process of sizing a wire driven by a repeater system. As shown in Fig.1, the minimum delay for a signal to propagate along an RLC line decreases while the power dissipation increases for wider interconnect. In this work tradeoff between signal propagation delay and transient power dissipation in sizing a long interconnect driven by a repeater system is discussed. Both line inductance and short-circuit power are considered.

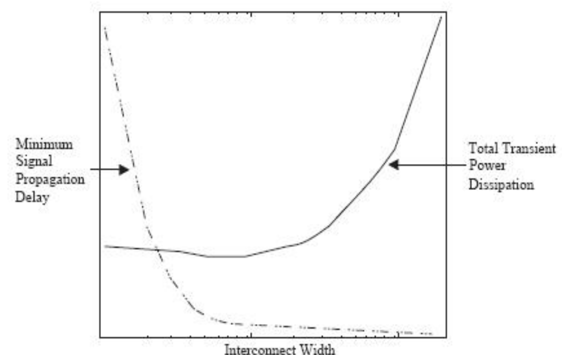

Fig.1. Minimum signal propagation delay and transient power dissipation as a function of line width for a repeater system.

II. REPEATER INSERTION SYSTEMS

The primary objective of a uniform repeater insertion system is to minimize the time for a signal to propagate through a long interconnect. Uniform repeater insertion techniques divide the interconnects into equal sections and employ equal size repeaters to drive each section as shown in Fig.2.

In some practical situations, the optimum location of the repeaters cannot be achieved due to physical space constraints. Changing the repeater size can compensate for a change in the ideal physical placement. Bakoglu and Meindl have developed closed-form expressions for the optimum number and size of repeaters to achieve the minimum signal

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propagation delay in an RC interconnect [7]. Adler and Friedman characterized a timing model for a CMOS inverter driving an RC load [8,9]. They used this model to enhance the accuracy of the repeater insertion process in RC interconnects. Alpert considered the interconnect width as a design parameter [10]. He showed that, for RC lines, repeater insertion outperforms wire sizing.

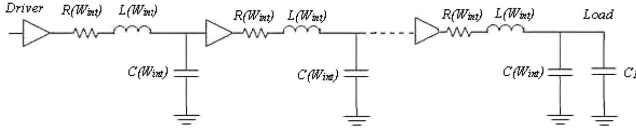

Fig. 2. Uniform repeater system driving a distributed RLC interconnects.

The delay can be greatly affected by the line inductance, particularly low-resistance materials with fast signal transitions. Ismail and Friedman extended previous research in repeater insertion by considering the line inductance [11]. They showed that on-chip inductance can decrease the delay, area, and power of the repeater insertion process as compared to an RC line model [12]. Interconnect sizing within a repeater system affects two primary design parameters, the number of repeaters and the optimum size of each repeater. Design criteria are developed to determine the optimum width, while considering different design objectives, such as the delay and power.

III. Analytical Modeling for Optimum Repeater Insertion

Traditionally, repeaters are inserted into RC lines to partition an interconnect line into shorter sections, e.g., [13], thereby reducing the total propagation delay. Applying the same idea to the general case of an RLC line, repeaters are used to divide the interconnect line into k sections as shown in Fig.3.

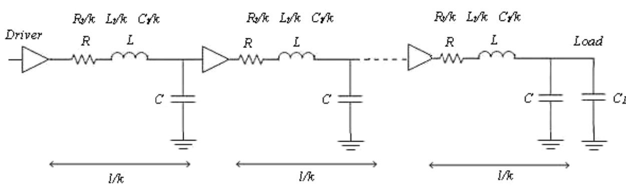

Fig. 3. Repeaters inserted in an RLC line to minimize the propagation delay.

The buffers are each uniformly the same size and h times larger than a minimum size buffer. The parasitic impedances R_t, L_t and C_t are given by $R_t=Rl$, $L_t=Ll$ and $C_t=Cl$ respectively, where R, L, and C are the resistance, inductance, and capacitance per unit length of the interconnect and l is the length of the line. The buffer output impedance R_{tr} is R_0/h and the input capacitance of the buffer C_L is hC_0. Where R_0 and C_0 are the minimum size buffer output resistance and input capacitance respectively.

The total propagation delay of the repeater system is the sum of the individual propagation delays of the k sections and is a function of h and k for a given interconnect line. The values of h and k at which the total delay $t_{pdtotal}$ a minimum is determined by simultaneously solving the following two differential equations [14],

$$\frac{\partial t_{pdtotal}(h,k)}{\partial h} = 0 \;\; \& \;\; \frac{\partial t_{pdtotal}(h,k)}{\partial k} = 0 \tag{1}$$

For the special case of an RC line $(L_t \to 0)$, the solution for these equations is

$$h_{opt}(RC) = \sqrt{\frac{R_0 C_t}{R_t C_0}} \;\; \& \;\; k_{opt}(RC) = \sqrt{\frac{R_t C_t}{2 R_0 C_0}} \tag{2}$$

Solving (1) for the general case of an RLC line is analytically intractable. Thus, the optimum number of sections k_{opt} and the optimum repeater size h_{opt} for an RLC interconnect is,

$$h_{opt} = \sqrt{\frac{R_0 C_t}{R_t C_0}} h^1(T_{L/R}) \;\; \& \;\; k_{opt} = \sqrt{\frac{R_t C_t}{2 R_0 C_0}} k^1(T_{L/R}) \tag{3}$$

where $h^1(T_{L/R})$ and $k^1(T_{L/R})$ are error factors that account for the effect of the inductance and $T_{L/R}$ is

$$T_{L/R} = \sqrt{\frac{L_t / R_t}{R_0 C_0}} \tag{4}$$

Curve fitting [14] is employed to determine a function that accurately characterizes h_{opt} and k_{opt}. These functions are

$$h_{opt} = \sqrt{\frac{R_0 C_t}{R_t C_0}} \frac{1}{\left[1 + 0.16 (T_{L/R})^3\right]^{0.24}} \tag{5}$$

$$k_{opt} = \sqrt{\frac{R_t C_t}{2 R_0 C_0}} \frac{1}{\left[1 + 0.18 (T_{L/R})^3\right]^{0.3}} \tag{6}$$

These closed form solutions are highly accurate with an error in the total propagation delay of the repeater system of less than 0.05% as compared to numerical analysis. These formulae can therefore be considered exact for all practical purposes. Thus, neglecting inductance not only increases the total delay of the repeater system but significantly increases the buffer area due to which power dissipation will be more. This trend is expected since treating interconnects as an RC line and neglecting inductance requires more repeaters.

IV. Total Power Dissipation for Repeater Systems

A. *Short-circuit power dissipation*

For wide interconnect, the short-circuit power increases as the line capacitance becomes dominant. Furthermore, increasing the length of the section by reducing the number of repeaters increases the short-circuit power of each section due to the higher section impedance.

The total short-circuit power [15] of a repeater system is

$$P_{sc-total} = k_{opt-RLC} P_{sc-section} \tag{7}$$

where

$$P_{sc-section} = \frac{1}{2} I_{peak} t_{base} V_{dd} f \tag{8}$$

where I_{peak} is the peak current that flows from V_{dd} to ground, t_{base} is the time period during which both transistors are on, V_{dd} is the supply voltage, and f is the switching frequency.

B. *Dynamic power dissipation*

The dynamic power is the power required to charge and discharge the various device and interconnect capacitances. The total dynamic power[15] is the summation of the CV^2f power from the line capacitance and the repeaters.

$$P_{dyn-total} = P_{dyne-line} + P_{dyn-repeaters} \tag{9}$$

where

$$P_{dyn-repeaters} = k_{opt-RLC} h_{opt-RLC} C_0 V_{dd}^2 f \tag{10}$$

$$P_{dyn-line} = C_{int} V_{dd}^2 f \tag{11}$$

$P_{dyn-repeaters}$ depend on both the number and size of each repeater. While the number of repeaters decreases, the repeater size increases. The dynamic power dissipated by a line increases with greater line capacitance (as the line width is increased). The dynamic power of the repeaters, however, decreases since fewer repeaters are used with wider lines. As shown in Fig. 4, the total dynamic power is a minimum for thin interconnect.

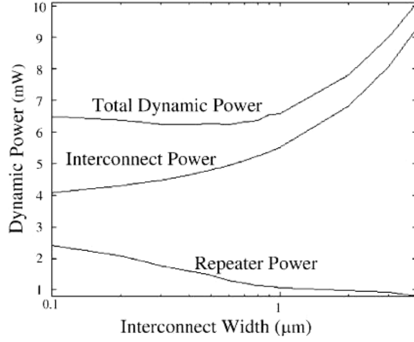

Fig. 4. Dynamic power dissipation as a function of interconnect width for l=20 mm.

C. Total power dissipation

In order to develop an appropriate criterion for determining the optimal interconnect width between repeaters, the total transient power dissipation of a system needs to be characterized. The total transient power can be described as

$$P_{total}(W_{int})=V_{dd}f\{k_{opt-RLC}(W_{int})[0.5I_{peak}(W_{int})\, t_{base}(W_{int})+h_{opt-RLC}(W_{int})V_{dd}C_0]+V_{dd}C_{int}(W_{int})\} \tag{12}$$

All of the terms in Eq.(12) are functions of the line width except V_{dd}, C_0, and f. Both transient power components decrease with increasing line width, thereby decreasing the total power until the line capacitance becomes dominant.

For an RLC interconnect, fewer repeaters are necessary to drive a line while achieving the minimum propagation delay. For an inductive interconnect, the line capacitance is typically larger than the input capacitance of the repeaters. Increasing the width reduces the power dissipation of the repeaters and increases the power dissipation of the line. The reduction in power dissipated by the repeaters overcomes the increase in the interconnect power until the line capacitance dominates the line impedance. After exceeding a certain width, the total power increases with increasing line width. The total power dissipation as a function of line width for different interconnect lengths is shown in Fig. 5 As the line width increases from the minimum width (i.e., 0.1. mm in the example technology), the total power dissipation is reduced. A minimum transient power dissipation therefore occurs with thin interconnect (see Fig. 5). The minimum transient power dissipation is obtained from

$$\frac{\partial P_{total}}{\partial W_{int}} = 0 \tag{13}$$

where $\partial P_{total} / \partial W_{int}$ is a nonlinear function of W_{int}. Numerical methods are used to obtain values of W_{int} for specific interconnect and repeater parameters.

Over a range of practical interconnect width, the total transient power increases as shown in Fig. 5. As the line length increases, the total power dissipation rapidly increases with increasing line width as the interconnect capacitance becomes dominant.

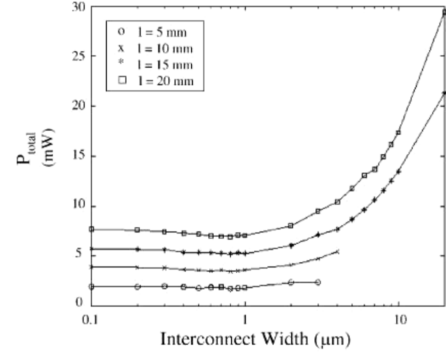

Fig. 5. Total transient power dissipation as a function of interconnect width.

To obtain optimum width, expressions for the line impedances which model the interconnecst are presented. Neglecting the line dielectric losses, a lossy transmission line is represented by the line resistance R, inductance L, and capacitance C, all per unit length.

$$R = \frac{\rho}{TW_{int}} \tag{14}$$

where, T, W_{int} are the line resistivity, thickness and width respectively.

Assuming a single line, C is given by,

$$\frac{C}{\varepsilon_{ox}} = 1.13\frac{W_{int}}{H} + 1.44\left(\frac{W_{int}}{H}\right)^{0.11} - 1.47\left(\frac{T}{H}\right)^{0.42} \tag{15}$$

L is the self-inductance of the line and is given by

$$L = 200\left[\ln\left(\frac{2l}{W_{int}+T}\right) + 0.5 + 0.22\left(\frac{W_{int}+T}{l}\right)\right] \tag{16}$$

Eq. (5) and Eq. (6) are verified for different value of interconnect length [0.25µm technology]as shown in Table.I. The number of section k_{opt} is compared for RC and RLC lines for various interconnect length as shown in Fig.6. The value h_{opt} is computed for different interconnect width as shown in Table.II and h_{opt} is compared for RC and RLC lines for various interconnect width as shown in Fig.7.

TABLE I: VALUE OF H_{OPT} AND K_{OPT} FOR DIFFERENT INTERCONNECT LENGTH.

l (mm)	R_t (Ω)	L_t (nH)	C_t (pF)	h_{opt} (RC)	k_{opt} (RC)	h_{opt} (RLC)	k_{opt} (RLC)
2	49.6	0.74	0.37	75	2	59	1
4	99.2	1.48	0.74	75	4	59	3
6	148.8	2.22	1.11	75	5	59	4
8	198.4	2.96	1.48	75	7	59	5
10	248	3.70	1.85	75	9	59	6

TABLE II: VALUE OF HOPT FOR VARIOUS INTERCONNECT WIDTH

w (µm)	R (Ω/cm)	L (nH/cm)	C (pF/cm)	h_{opt} (RC)	h_{opt} (RLC)
0.9	494	4.75	1.73	51	44
1.8	248	3.70	1.85	75	59
2.4	76	5.30	2.60	160	79
7.5	35	3.47	5.16	333	145

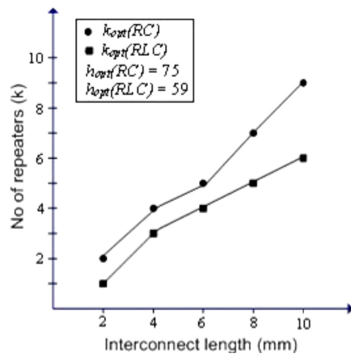

Fig.6. Comparison of k_{opt} for RC and RLC lines

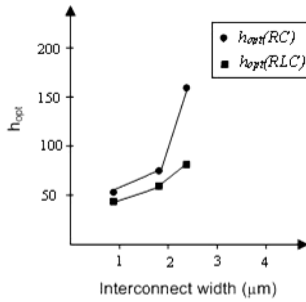

Fig..7. Comparison of h_{opt} for RC and RLC lines

For certain interconnect parameters [0.25μm technology] transient power dissipation for various interconnect length is as shown in Table.III.

TABLE III: TOTAL TRANSIENT POWER DISSIPATION FOR DIFFERENT INTERCONNECT LENGTH.

l(mm)	W_{INT}(μm)	No. of repeaters	Repeater size	Total power (mW)
5	0.8	1	43.3	1.73
15	0.8	5	43.2	5.2

Thus, neglecting inductance not only increases the total delay of the repeater system but significantly increases the buffer area due to which power dissipation will be more. This trend is expected since treating the interconnect as an RC line and neglecting inductance requires more repeaters.

V. CONCLUSION

In this work analytical expressions are derived for optimum buffer or repeater insertion for optimized width to reduce both delay and power during interconnect optimization for high complex SoC design. For a long inductive interconnect line, an optimum interconnect width exists that minimizes the total transient power dissipation. A closed form solution is presented for determining this optimum width. These algorithms can be implemented in an future VLSI EDA tool which helps to optimize the delay and power during global interconnects optimization after design layout and routing has been done.

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