Statistical Approach to Design Low Noise Amplifier

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***Abstract*—CMOS transistors have been consistently scaled to smaller feature sizes and continue to reduce towards sub-0.1 um lengths. However, as the channel length decreases, so does the gate oxide thickness, dictating a decrease in the supply voltage. Driven by the needs for low power, small size and low cost, CMOS radio frequency integrated circuits (RFIC) design becomes main stream in modern portable wireless communications. The ultimate goal in RFIC design is to having battery-less systems so as to decrease power dissipation. Commonly a Low Noise Amplifier (LNA) is a key component is RF front end receiver which poses a challenge in terms of meeting high gain, low noise figure, good linearity and low power consumption requirement. The primary role of the LNA is to lower the overall noise figure of the entire RF front end, noise optimization is considered as one of the most critical steps in the LNA design procedure. A 0.7V, 1GHz low noise amplifier has been designed and simulated using spectre simulator in a standard TCMC 0.18um CMOS technology. With low power noise optimization techniques, the amplifier provides the gain of 23dB, a noise figure of only 1.1dB, power dissipation of 8.4mw from 0.7v power supply.**

***Index Terms*—Low Noise Amplifier (LNA), Noise Figure (N.F), Radio Frequency (RF) and CMOS.**

I. Introduction

Recently has been much interest in using CMOS for RF ICs operating in the 900MHz to 2.5GHz. This frequency range is used by cellular phone applications such as GSM (Global system for Mobile Communication), and cordless application such as DECT (Digital Enhanced Cordless Telecommunications). Commonly a low noise amplifier (LNA) is a key component in RF front-end receiver which poses a challenge in terms of meeting high gain, low noise figure and linearity requirement at sub 1 Volt power supply (such as 0.7V). The primary role of the LNA is to lower the overall noise figure of the entire RF front-end, noise optimization is considered as one of the most critical steps in the LNA design procedure.

The noise figure (NF) of LNA should not exceed a 3 dB, assuming it has a gain more than 10 dB [1]. The design of LNA is full trade-offs between optimum gain, lowest noise figure, high linearity and low power consumption. Cascode topology is one of the most popular topology used for CMOS LNA design, which provides high gain, low noise, but it is not suitable for sub 1V power supply. Statistical modeling and improvement procedure for RF design is illustrated in section II. The consideration for noise optimization of LNA is described in section III. The proposed LNA design suitable for sub 1V power supply is analyzed in Section IV. Spectre simulation results and a comparison with other reported LNAs are presented in Section V. Section VI concludes the paper.

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II. Statistical Modeling and Improvement for RF Design

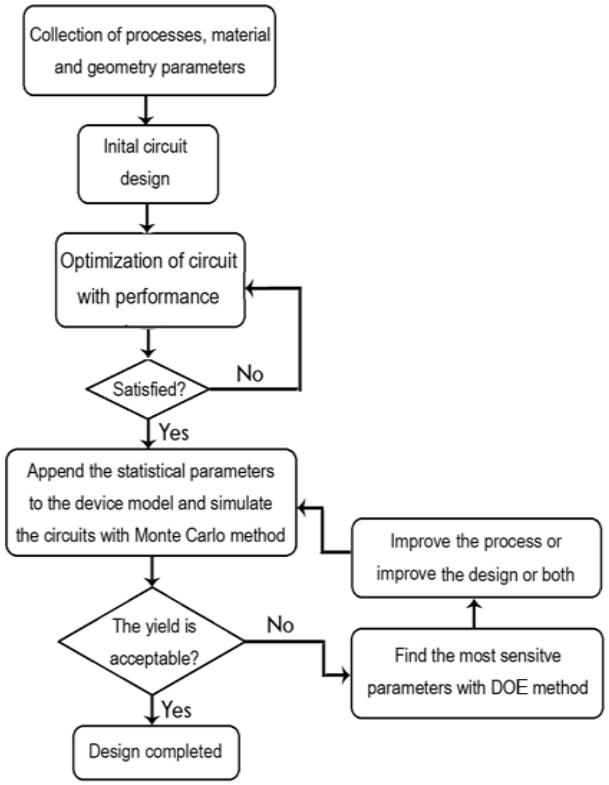
Statistical analysis of RF design begins from modeling of the component in the module.

Generally, the methods for device modeling can be classified into two categories: equivalent circuit-based models (ECMs) and physics based models (PBMs). ECM modeling assumes an equivalent circuit to simulate the external behavior of the device under consideration. ECM has high computational efficiency and is relatively easy to be implemented into circuit simulators. However, since the model parameters are usually identified after device fabrication, they have limited extrapolative or statistically meaningful forecasting abilities. PBMs address the fundamental device equations and characterize device behavior in terms of physical parameters. Especially, passive components could be modeled with such parameters easily. Circuit analysis can be performed at the device parameter level. Thus, in our statistical modeling of RF SoP module, PBM is implemented.

RF SoP module, PBM is implemented. Each component in SoP module is modeled with an equivalent circuit which contains information of the geometry parameters (such as the wire widths, wire space), process parameters (such as the thickness of interlayer dielectrics, conductor thickness) and material parameters (such as dielectric constant, resistivity of conductor). The statistics of those parameters (including variation range, distribution function, etc) are also collected and are appended to the initial models of the components. The circuits are designed with these components [9].Statistical responses of the components and the RF SoP modules are studied through Monte Carlo method. If the yield of the circuits obtained from the statistical analysis is not good enough, optimization of the circuits should be implemented in next step. The most sensitive parameters (which contribute most significantly to the variation of response of the circuits) are found firstly.

Design of Experiment (DOE), a widely used systematic method for experiment planning, is applied to find the most sensitive parameters. Based on the number of variables and accuracy requirement of the model, the level and the method of experiment can be chosen. The level of an experiment is

the number of values that each input variable will be assigned to during the experiment. With DOE analysis, the most sensitive parameters are found. Then, the circuits are improved with the following ways: 1) improving the manufacturing process and material quality to make the distribution of these sensitive parameters more concentrated; 2) improving the circuit design to make these parameters with less contribution to the response of the circuits. Improving process may not be available in most cases because of the limitation of technology and the cost. A better way is to improve through design. In the designs, parameters which contributed mostly to the variation of circuit response were desensitized.



Flow Chart of the Statistical analysis procedure optimization

The optimization methods are specified to each of the parameter.

A flowchart of the statistical analysis procedure described above.

III. Noise Figure And Optimization

A. Noise figure

An LNA determines the performance of the communication systems. It needs higher linearity and sufficient gain to overcome the next stage noise but not to overload. A system noise factor is defined as:

$$F = \frac{N_{in} + \sum_{k=1}^{n} N_{ai,k}}{N_{in}} = F_1 + \frac{F_2 - 1}{A_1^2} + \frac{F_3 - 1}{A_1^2 A_2^2} + \ldots (1)$$

where F_n(n=1,2,3,….) is the noise factor of each stage, A_n (n=1,2,3…) is the gain of each stage. In our circumstances, F1 is the noise of the LNA and A1 is the gain of the LNA will lower the total noise of the system. Noise figure represents how much the given system degrades the signal-to-noise ratio, which is defined as;

$$NF = 10\log \frac{total\ \ output\ \ noise\ \ power}{output\ \ noise\ \ power\ \ due\ \ to\ \ input\ \ source} (2)$$

CMOS LNA design provides high level of integration at low cost but it is a big challenge to achieve low noise performance because of the noisy nature of MOS device. The dominant noise source in MOS devices is channel noise: [2]

$$i_{nd}^{\ 2} = 4kT\gamma g_{d0} \quad (3)$$

where g_{do} is the zero-bias drain conductance of the device. γ is a bias dependent factor which, for long channel device satisfies $\frac{2}{3} \le \gamma \le 1$, but for short channel devices can be as large as two or three, depending on bias condition. Another source of noise in MOS devices is the noise generated by the distributed gate resistance. This noise can be modeled by a series resistance in the gate circuit and an accompanying with noise generator, which results in:

$$v_{rg}^{\ 2} = 4kT\delta r_g \Delta f \quad (4)$$

where δ is the coefficient of gate noise, normally equal to 4/3 for long channel devices and r_g is the gate resistance. The gate resistance can be minimized through interdigitation without the need of increased power dissipation, thus it is rendered insignificant [2]. If the sizes of the MOS transistors are carefully chosen, the optimum ω_t which is simply a ratio of g_m /C_{gs} can be obtained. Therefore, the minimum noise figure can be achieved according to [3]:

$$F_{min} = 1 + \frac{w}{w_t}\sqrt{\gamma\delta\zeta(1 - |c|^2)} \quad (5)$$

If δ were zero, the minimum noise figure would be 0dB[4].

B. Noise Optimization

To achieve lower noise and higher gain, the Common-source with the inductor degeneration topology is employed and shown in Fig. 1.

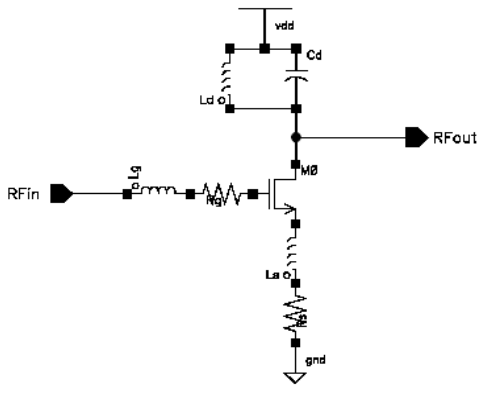


Fig. 1.Iinductive Ly Degenerated Common Source Amplifier

Neglecting the gate drain capacitances, the input impedance of the LNA shown in Fig1 is: [4]

$$Z_{in} = \frac{g_m L_s}{C_{gs}} + \frac{1}{C_{gs} S} + S(L_S + L_g) + R_g \quad (6)$$

where g_m and C_{gs} are the transconductance and the gate-to source capacitance of the input device M0 respectively. L_g

and L_s are the gate and source inductors and R_g is the effective gate resistance of M_0 given by: $R_g=R_0/(3n^2L)$.
where R_0 is the sheet resistance of the gate polysilicon, W and L are the gate width and length of the transistor M_0 respectively and n is the number of fingers [2].
At the resonant operating frequency (w_0), the input matching requires that:

$$Z_{in} = R_s = \omega_t L_s \quad (7)$$

The C_{gs} source degeneration inductance L_s is chosen together with ω_t to provide the desired input resistance Rs, the real term can be made equal to 50 ohm without the existence of a real noisy resistor. Then, the input impedance of the LNA is matched to source resistance R_s when the above condition is met.

IV. Design Approach

To make the LNA works at 0.7V, the well-Source junction of the NMOS transistors are forward biased which causing the threshold voltage to decrease. The threshold voltage with body effect is based on the following expression.

$$V_{TO} + \gamma[\sqrt{2\phi_f - V_{BS}} - \sqrt{2\phi_f}] \quad (8)$$

Which, V_{TO} the intrinsic threshold voltage, γ the body effect coefficient, ϕ_f the surface inversion potential of silicon and V_{BS} the bulk-source voltage. By applying a voltage on V_{BS} we can control the threshold voltage V_T and thus the polarization of the transistor. In this LNA design, the V_T can be decreased from 0.5V to 0.4V and the value of current through bulk is 10 uA although this current is undesirable. For LNA design, inductive source degeneration is used to achieve good input matching without adding thermal noise introduced by real resistor. The proposed topology is shown in Fig.3.

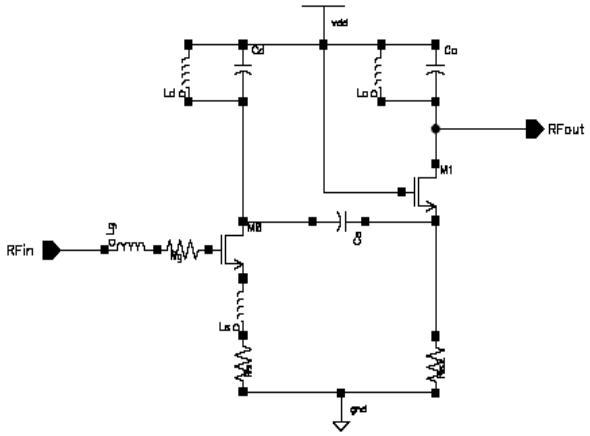


Fig.2. Common Source Common Gate Topology

Which works for sub 1 volt low power supply applications, in our case it is 0.7V? Inductive source degeneration is used to achieve good input matching and reduce noise figure. The first stage is inductively degenerated common-source amplifier formed by transistor M_0. Followed by a common-gate configurated transistor M_1. The value of LC tank of M_0 is carefully chosen to achieve a resonance frequency of 1GHz and is required to have a much higher impedance than that of the input impedance looked at the source of M_1. It provides a DC bias current path and a high impedance branch to force the RF signal to flow into the source of M_1 through a big DC coupling capacitance C_s

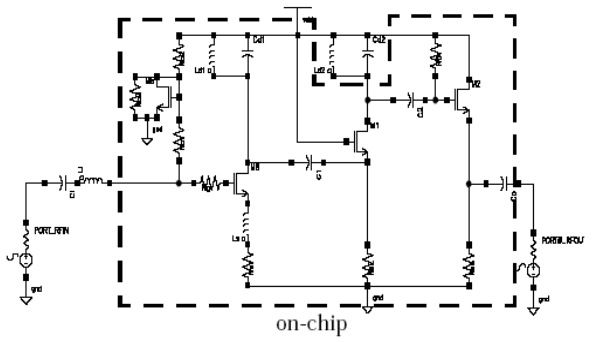


Fig.3.Complete Schematic of Proposed Common-Soure, Common-Gate LNA

The input impedance of the LC tank (L_d,C_d) is

$$Z_d = R_d + \frac{\omega^2 L_d^2}{R_d} \approx \frac{\omega^2 L_d^2}{R_d} = R_d Q_d^2 \quad (9)$$

Then,

$$g_{m1} \gg \frac{1}{R_d Q^2 d} \quad (10)$$

If R_L << r_{ds}, where R_d and Q_d are the resistance and the quality factor associated with the inductor L_d.
The input impedance at the source of the common gate transistor M_1 is:

$$R_i = \frac{1}{g_{m1} + g_{mb1}} \approx \frac{1}{g_{m2}} \quad (11)$$

where g_{mb} is the bulk transconductance.

V. Simulation Results

The complete circuit is shown in Fig 4. The LNA first stage M0 is inductively degenerated representing this common source amplifier followed by M1 configured as common-gate device. Mb sets the dc bias for M0. M2 is configured as the buffer stage for LNA output matching. C1 between M0 and M1 is acting as a DC coupling capacitance to block DC and provides ac path to let RF signal flow into the source of common gate transistor M1. In our case, it is designed to be 10 pF. Inductors which are smaller than 5 nH are placed on chip otherwise, they are off-chip. As shown in Fig4 only the framed components are on-chip.

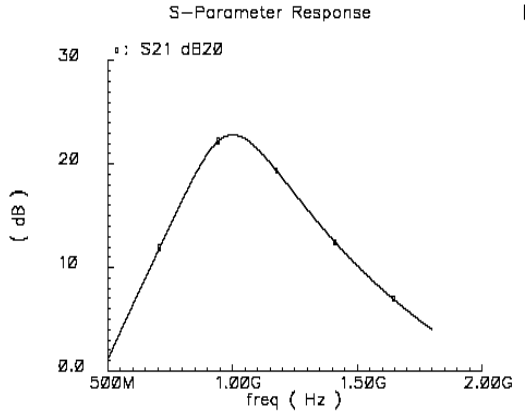


Fig.4. power gain of proposed LNA

The proposed circuit was simulated using Spectre simulator in 0.18um CMOS process. After noise optimization a low noise figure of 1.1 dB at 1 GHz is achieved and shown in Fig 5.

The S-parameters of the LNA are illustrated in Fig 4, 6, 7, and 8. Figure 4 shows a forward power gain (S21) of 23 dB at 1 GHz. The S11 shows a good input match at -13.5dB.The S22 shows a good output match with the output buffer which achieves -21dB.The S12 shows a low reverse transmission which is 72dB. The IIP3 simulation result of the LNA is shown in Figure 9. A two-tone signal which is chosen close to each other has been applied to the input port. The input-referred third-order intercept points (IIP3) is -29dBm. The layout of the LNA is shown in Fig 9. The chip area is 0.9mm x 0.9mm. This work is placed alongside

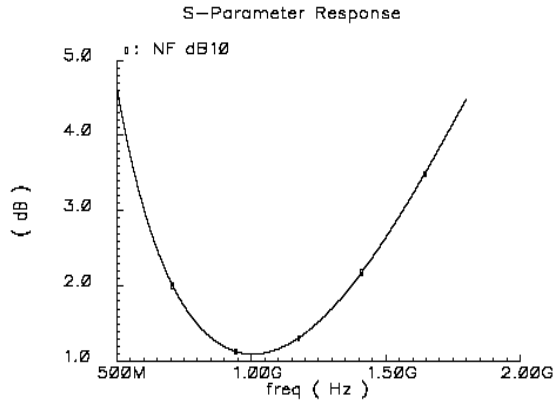


Fig.5. Noise figure of proposed LNA

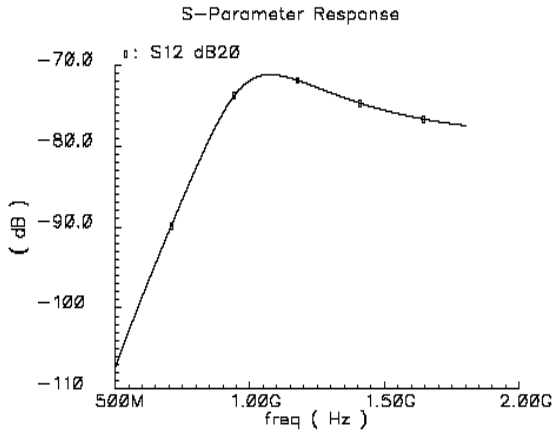


Fig. 6. S12 of proposed LNA

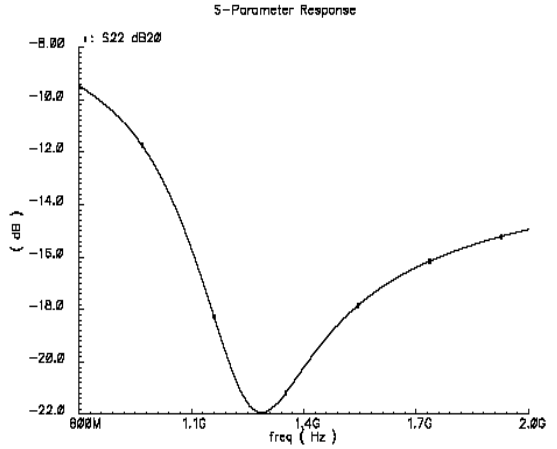


Fig.7. S22 of proposed LNA

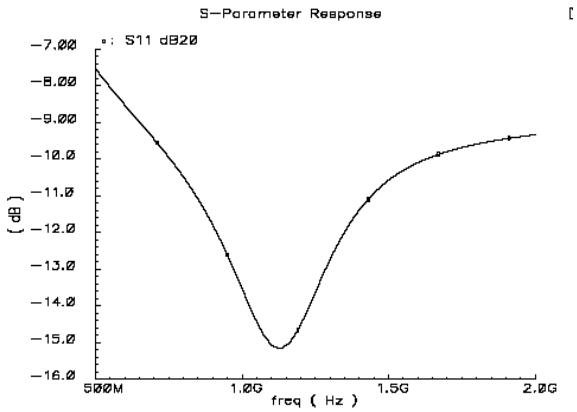


Fig. 8. S11 of proposed LNA

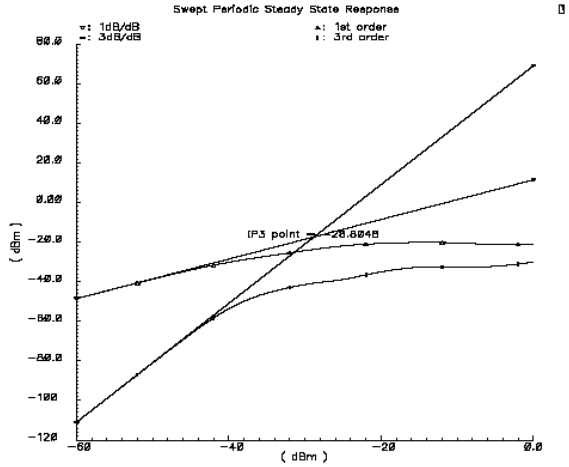


Fig.9. IIP3 Simulation of the proposed LNA

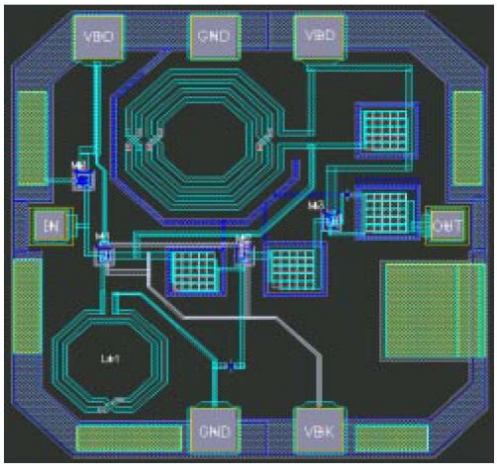


Fig.10.layout of the proposed LNA

TABLE I: COMPARISON OF VARIOUS RECENT REPORTED LNAS

Reference	[5]	[6]	[7]	[8]	[1]	This Work
Freq(G Hz)	0.9	0.9	0.9	1	1	1
NF(dB)	2	2.5	6	3.5	2.7	1.1
S_{21}(dB)	17.5	9	17	22	12.2	23
$IIP_{3(dBm)}$	-6	-4.7	-14	12	-21	-29
Power(mw)	-	10	78	27	17	8.4
Tech(um)	0.35	0.5	0.8	1.0	0.5	0.18

With other recent reported LNA in Table 1. It shows that with the noise optimization techniques the proposed LNA achieve a much lower noise figure than other LNAs.

VI. Conclusions

In this paper, a new CMOS low noise amplifier using common-source inductive source degeneration followed by common-gate configurations is proposed. The proposed topology is suitable for low power supply application and works good at 0.7 V voltage supply. Spectre simulation using TSMC 0.18μm CMOS technology shows a low noise figure of 1.1 dB, high power gain (S21) of 23 dB and low power consumption of 8.4 mW from 0.7 V power supply.

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