International Journal of Computer and Electrical Engineering, Vol. 3, No. 2, April, 2011
1793-8163

A Low Voltage, High Quality Factor Floating Gate Tunable Active Inductor with Independent Inductance and Quality Factor Tuning

Mahdi Ebrahimzadeh

***Abstract*—A CMOS active inductor that has a large quality factor and independent *L* and *Q* tuning capability is presented. The tunable active inductor has 0.8 V supply voltage. In this voltage this TAI shows a quality factor equal to 11400 and power dissipation of 1.8 mW. It has 1.4 GHz inductive bandwidth. The TAI has an interesting property that has an independent inductance and quality factor tuning.**

***Index Terms*—Low voltage, floating gate, active inductor, high quality factor**

I. Introduction

CMOS active inductors have found increasing applications in areas where an inductive characteristic is required. These applications include *LC* oscillators, RF bandpass filters, RF phase shifters, limiting amplifiers for optical communications, low noise amplifiers for wireless communications, RF power dividers, ultra wideband low noise amplifiers, and transceivers for high-speed data links over wire lines. These components have some attractive advantages such as low silicon area consumption, large and tunable inductance, large and tunable quality factor, large and tunable self resonance frequency and compatibility with digital CMOS technologies. However, active inductors have some disadvantages compared to spiral inductors that limit their use in RFIC and MMIC designs such as their higher noise, nonlinear behavior, power dissipation, sensitivity to process, and voltage and temperature variations [1]. Moreover, most of published tunable active inductor designs suffer from one major drawback, which is their inability to independently control both the TAI inductance and quality factor [2,3,4].

Application for radio frequency communication system on a chip (SoC) need for low power low voltage integrated high frequency filters and oscillators. Using floating gate we can reduce the active inductor supply voltage and in consequence reduce the power dissipation from it. Moreover adding the feedback resistance allows us to independently control over *L* and *Q* and to enhance the *Q* of TAI. The effect of adding the feedback resistance is analyzed and design equations are presented. It will be shown that this gyrator-C architecture allows independent control over *L* and *Q*. In this paper these two techniques are used to improve performance of tunable active inductor in low voltage, low power behavior and to have independency between tuning *L* and *Q*.

This paper is organized into four sections. Section II covers design and analysis of high *Q* TAI with independent tuning *L* and *Q*. Section III presents the simulation results and comparison with other related works. Section IV is about noise analysis of the design, followed by the conclusion in section V.

Manuscript received April 10, 2010.

Mahdi Ebrahimzadeh is with the Electrical Engineering Department, Iran University of Science and Technology (corresponding author to provide phone: +98-021-84977579; fax: +98-021-77240486; e-mail: mahdi.ebrahimzadeh@gmail.com).

II. Active Inductor Design

The most common active inductor topology is grounded active inductor. This circuit topology is based on gyrator theory containing two or more transistors to generate an inductive impedance. When one port of the gyrator is connected to a capacitor, as shown in Figure.1, the network is called the gyrator-C network and base on (1) could make an active inductance. This architecture of active inductors can obtain several nH of inductance that operate at a few GHz region.

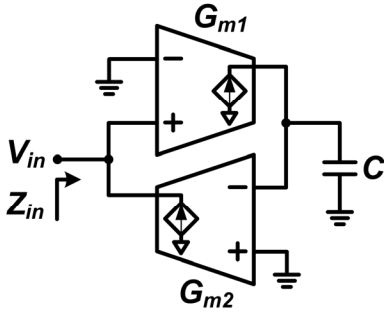
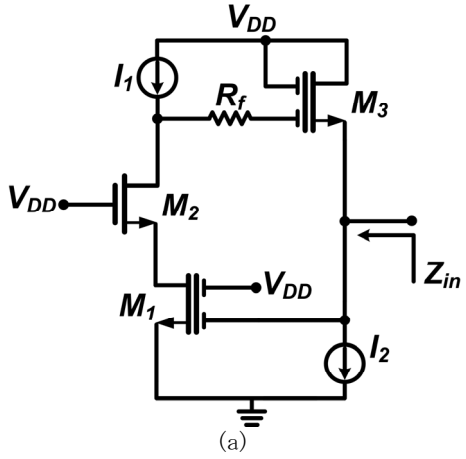


Figure 1. Active inductors based on Gyrator-C networks

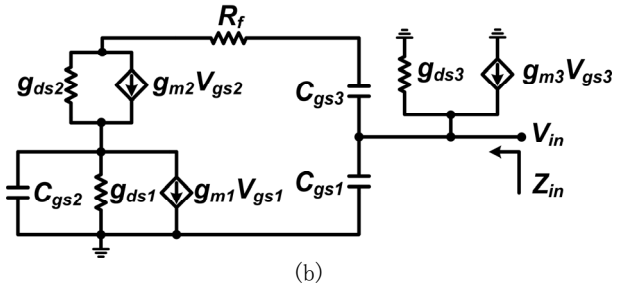
$$Z_{in} = \frac{sC}{G_{m1}G_{m2}} \Rightarrow L = \frac{C}{G_{m1}G_{m2}} \quad (1)$$

For achieving a higher inductance and a higher quality factor, a cascode circuit topology has been used to reduce the output conductance by CMOS technologies. Moreover using floating gate technique allows us to lower active inductor's supply voltage to have a low voltage low power design. Adding a feedback resistance to the gyrator-C architecture generates a negative resistance necessary to enhance the TAI's *Q*. The active inductor and its equivalent circuit are shown in Figure.2, where the resistance R_f is the additional

feedback resistance.



(a)



(b)

Figure 2. a) Floating gate active inductor using Rf feedback, b) It's high frequency equivalent circuit.

The expression for the input impedance of this gyrator-C architecture is:

$$Z_{in}=\frac{s^2\left(C_{gs2}C_{gs3}\right)\left(1+R_f g_{ds2}\right)}{A(s)}+\ldots$$
$$\frac{s\left(g_{ds2}C_{gs2}+R_f C_{gs3}g_{ds1}g_{ds2}+C_{gs3}g_{ds1}+C_{gs3}g_{ds2}-g_{m2}C_{gs3}\right)+g_{ds1}g_{ds2}}{A(s)} \quad (2)$$

That

$$A(s)=s^3\left(C_{gs1}C_{gs2}C_{gs3}\right)\left(1+R_f g_{ds2}\right)+s^2(C_{gs1}(g_{ds2}C_{gs2}+R_f C_{gs3}g_{ds1}g_{ds2}$$
$$+C_{gs3}g_{ds1}+C_{gs3}g_{ds2}-C_{gs3}g_{m2})+g_{ds2}C_{gs2}C_{gs3}+\left(1+R_f g_{ds2}\right)\left(g_{ds3}C_{gs2}C_{gs3}\right))$$
$$+s(g_{ds1}g_{ds2}C_{gs1}+g_{m3}g_{ds2}C_{gs2}+g_{ds1}g_{ds2}C_{gs3}+g_{m1}g_{ds2}C_{gs3}-g_{m1}g_{m2}C_{gs3}$$
$$+g_{ds3}(g_{ds2}C_{gs2}+R_f C_{gs3}g_{ds1}g_{ds2}+C_{gs3}g_{ds1}+C_{gs3}g_{ds2}-C_{gs3}g_{m2}))$$
$$+g_{ds1}g_{ds2}g_{ds3}+g_{ds1}g_{ds2}g_{m3}+g_{m1}g_{m3}g_{ds2}-g_{m1}g_{m2}g_{m3} \quad (3)$$

It seems that this equation to be very cumbersome. It shows that adding the feedback resistance R_f to the gyrator-C loop adds a zero and a pole to the input impedance transfer function, which allows more control over the frequency response of the TAI. Specifically, the additional zero in the input impedance transfer function generates a negative term that can be used to enhance the TAI's Q.

To understand more how Q-enhancement and independency over L and Q take place, the circuit is modeled by the L-C circuit shown in Figure. 3. It can be shown that the impedance of the inductive branch (Zp), given by the series combination of the equivalent inductance L and equivalent series resistance R_S, is expressed as:

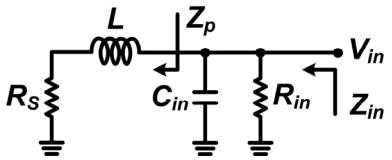


Figure 3. Equivalent LC model of TAI

$$Z_p=\frac{s^2\left(C_{gs2}C_{gs3}\right)\left(1+R_f g_{ds2}\right)}{g_{m1}g_{m2}g_{m3}}+\ldots$$
$$+\frac{s\left(g_{ds2}C_{gs2}+R_f C_{gs3}g_{ds1}g_{ds2}+g_{ds1}C_{gs3}+g_{ds2}C_{gs3}-g_{m2}C_{gs3}\right)+g_{ds1}g_{ds2}}{g_{m1}g_{m2}g_{m3}} \quad (4)$$

So, the equivalent inductance (L) and the equivalent series resistance (R_S) are expressed as:

$$L=\frac{\left(g_{ds2}C_{gs2}+R_f C_{gs3}g_{ds1}g_{ds2}+g_{ds1}C_{gs3}+g_{ds2}C_{gs3}-g_{m2}C_{gs3}\right)}{g_{m1}g_{m2}g_{m3}} \quad (5)$$

And

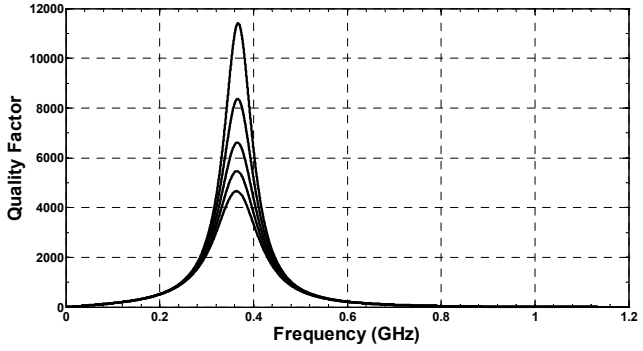
$$R_S=\frac{g_{ds1}g_{ds2}-\omega^2\left(C_{gs2}C_{gs3}\right)\left(1+R_f g_{ds2}\right)}{g_{m1}g_{m2}g_{m3}} \quad (6)$$

(5) indicates that the inductance is independent of the feedback resistance as long as the feedback resistance is much smaller than the output resistance r_{o1} ($1/g_{ds1}$) of the M_1 transistor. On the other hand, (6) indicates that, R_S can be reduced and take negative values, and its value can be controlled via the feedback resistance R_f. Furthermore, controlling R_S via R_f does not affect L (assuming $r_{o1}>>R_f$), which consequently allows us to independently tune L and Q.

III. Simulation Results

This active inductor was simulated by 0.18 µm TSMC RF CMOS designkit in ADS simulator, and all transistors, M_1, M_2 and M_3, have 50µm channel width to provide sufficient C_{gs}, g_{ds} and g_m. For simulation of quality factor we use its basic definition $Q=Im(Z_{in})/Re(Z_{in})$. This parameter was simulated using S-parameter simulation in ADS.

The designed TAI was simulated in two manner tuning. The first tuning generates variable peak Q value and fixed L value and the second generates a variable L value and fixed peak Q value. These results are shown in Figure.4 and Figure.5.



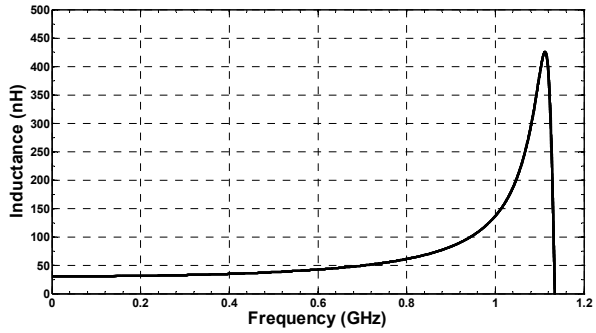


Figure 4. Fixed L and variable peak Q value

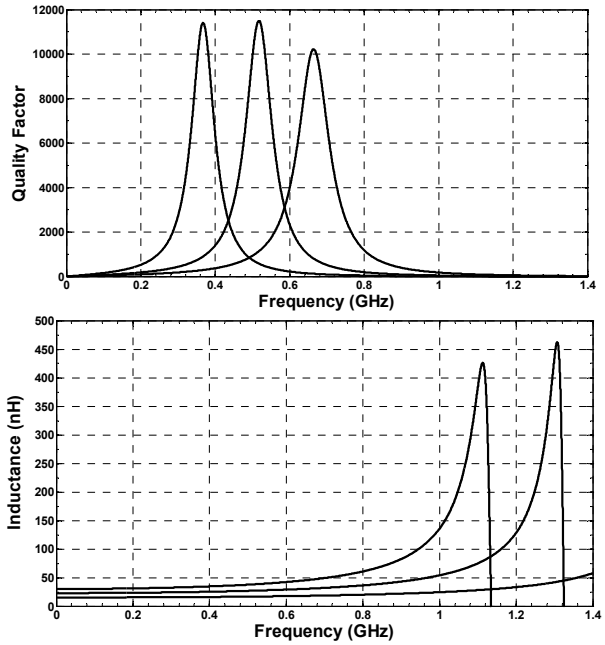
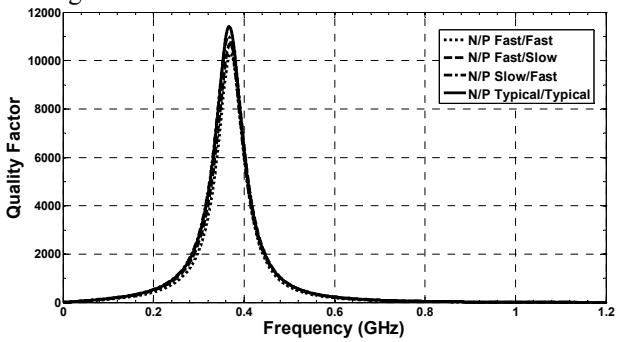


Figure 5. Fixed peak Q value and variable L

As shown in Figure.4 varying the peak *Q* value does not change the value of inductance and pursuant to Figure.5 varying the value of inductance does not change the peak *Q* value of TAI.

Some of most important specifications of this TAI are compared to other related works in TABLE I. This comparison is based on these specifications toward low voltage high *Q* active inductors.

The effect of process variations on the performance of the active inductor is investigated using corner case technologies of TSMC RF CMOS 0.18 µm. The results are shown in Figure.6. For these simulations we performed a few tuning in the design.



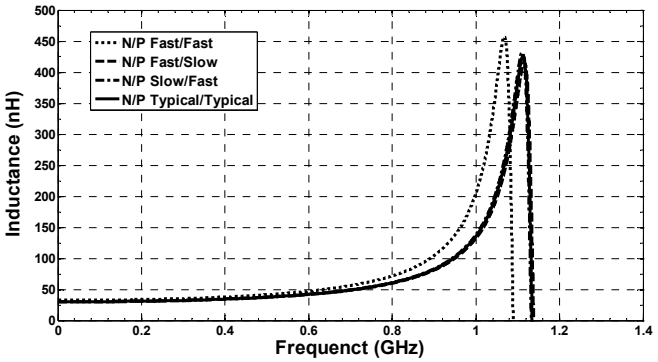


Figure 6. Worst Case simulation of the TAI

IV. TAI Noise Analysis

This section analyzes the noise generated by the TAI circuit due to the various transistors as well as the feedback resistor R_f. Our goal is to find an equivalent noise voltage source (v_{nL}), which can be connected in series to the TAI circuit to model the effect of the various noise sources. In this analysis, the effect of the flicker noise generated by the transistors is neglected, since for RF applications the design frequency is well above the 1/*f* corner frequency. Therefore, only the thermal noise components are considered.

A simplified schematic of the TAI circuit with the different noise sources is shown in Figure. 7, where i^2_{nk} is the mean-square value of the drain current thermal noise generated by transistor M_k, and v^2_{nRf} is the mean-square value of the thermal noise voltage generated by the feedback resistance R_f. For simplicity, the gate noise is neglected throughout this analysis as well as the output resistances $r_{o1,2}$, and the gate-source capacitances $C_{gs1,2}$ of transistors M_1 and M_2. Assuming all the various noise sources are uncorrelated, one can use superposition to show that, the mean-square value of the input referred noise voltage (v_{nL}) at the inductor input port is expressed as:

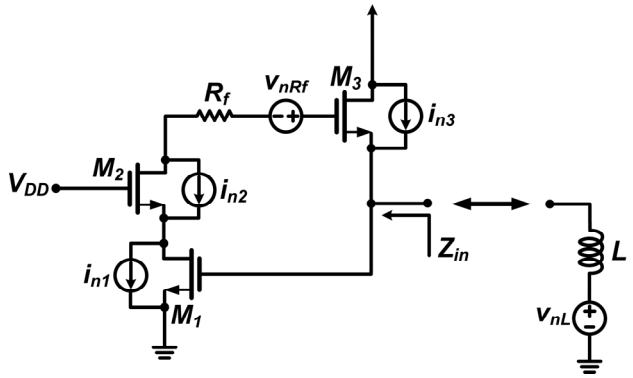


Figure 7. TAI schematic with the main current and voltage noise sources, and equivalent lumped noise voltage model

TABLE COMPARISON OF MOST IMPORTANT SPECIFICATIONS OF TAI WITH OTHER RELATED WORKS

	[5]	[6]	[7]	[8]	[9]	[10]	This Work
Technology	0.18 µm CMOS	0.35 µm CMOS	0.35 µm CMOS	0.35 µm CMOS	0.13 µm CMOS	90 nm CMOS	0.18 µm CMOS
Inductive Bandwidth	2 GHz	1.6 GHz	1.9 GHz	2.9 GHz	7 GHz	12.5 GHz	1.4 GHz
L (nH)	60	40	320	31	38	NA	42
Q_{max}	70 *	260	50	434	3900	635	11400
Supply Voltage (V)	2	1.5	1.5	1.5	1.2	0.9	0.8
Power (mW)	8	2	NA	0.6	1	NA	1.8

*Measured

$$v_{nL}^2 = r_{o1}^2 i_{n1}^2 - r_{o2}^2 i_{n2}^2 - r_{o1}^2 C_{gs3}^2 \omega^2 v_{n,Rf}^2 - r_{o2}^2 C_{gs3}^2 \omega^2 v_{n,Rf}^2 + R_f^2 r_{o1}^2 C_{gs3}^2 \omega^2 i_{n2}^2 - R_f^2 r_{o2}^2 C_{gs3}^2 \omega^2 i_{n2}^2 + r_{o1}^2 r_{o3}^2 C_{gs3}^2 \omega^2 i_{n3}^2 - r_{o1}^2 r_{o3}^2 C_{gs1}^2 \omega^2 i_{n1}^2 + r_{o1}^2 r_{o3}^2 C_{gs3}^2 \omega^2 i_{n1}^2 + r_{o2}^2 r_{o3}^2 C_{gs3}^2 \omega^2 i_{n3}^2 + r_{o2}^2 r_{o3}^2 C_{gs1}^2 \omega^2 i_{n2}^2 - r_{o2}^2 r_{o3}^2 C_{gs3}^2 \omega^2 i_{n2}^2 + r_{o1}^2 r_{o2}^2 C_{gs2}^2 \omega^2 i_{n2}^2 / r_{o1}^2 C_{gs3}^2 \omega^2 - r_{o3}^2 C_{gs1}^2 \omega^2 + r_{o3}^2 C_{gs3}^2 \omega^2 - r_{o1}^2 C_{gs2}^2 \omega^2 + r_{o2}^2 C_{gs3}^2 \omega^2 + R_f^2 C_{gs3}^2 \omega^2 + 1 \quad (7)$$

The noise performance simulation of the circuit is given in Figure. 8 which proves to be low in comparison with related works [9]. The results of this analysis can be used to quantify the noise performance of the TAI-based RFICs such as LNAs, LC oscillators, phase shifters and so on.

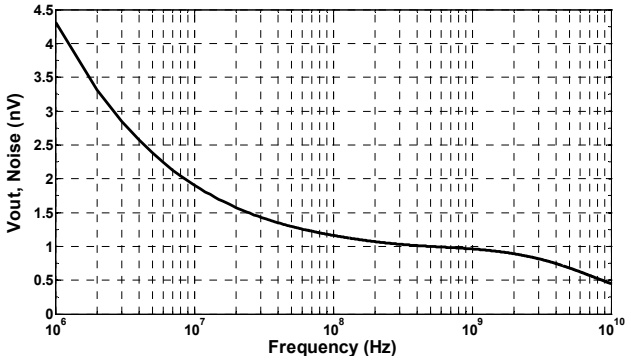


Figure 8. Noise performance of the active inductor

V. Conclusion

A low voltage high quality factor floating gate active inductor was presented. This design has the capability of independent tuning of inductance value and quality factor. Adding the feedback resistance allows us to enhance the TAI quality factor and independently tune inductance value and quality factor of the active inductor. The TAI simulated using TSMC RF 0.18 µm CMOS technology. It has quality factor equal to 11400 at 0.8 V supply voltage and 1.8 mW power dissipation.

Acknowledgements

The author would like to thank the Iran Communication Research Centre for the financial and technical support.

References

[1] F. Yuan, *CMOS Active Inductors and Transformers Principle, Implementation, and Applications*. New York: Springer, 2008.

[2] Leifso, C. ; Haslett, J.W. ; McRory, J.G., "Monolithic tunable active inductor with independent Q control," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, no. 6, pp. 1024-1029, Jan. 2000.

[3] Mukhopadhyay, R. ; Yunseo Park ; Sen, P. ; Srirattana, N. ; Jongsoo Lee ; Chang-Ho Lee ; Nuttinck, S. ; Joseph, A. ; Cressler, J.D. ; Laskar, J., "Reconfigurable RFICs in Si-based technologies for a compact intelligent RF front-end," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 1, pp. 81-93, Jan. 2005.

[4] Abdalla, M.A.Y. ; Phang, K. ; Eleftheriades, G.V., "Printed and Integrated CMOS Positive/Negative Refractive-Index Phase Shifters Using Tunable Active Inductors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 55, no. 8, pp. 1611-1623, Aug. 2007.

[5] Chao-Chih Hsiao ; Chin-Wei Kuo ; Chien-Chih Ho ; Yi-Jen Chan, "Improved quality-factor of 0.18-µm CMOS active inductor by a feedback resistance design," *IEEE Microwave and Wireless Components Letters*, vol. 12, no. 12, pp. 1531-1309, Dec. 2002.

[6] Sae-Ngow, S. ; Thanachayanont, A., "A low-voltage, wide dynamic range CMOS floating active inductor," *TENCON 2003. Conference on Convergent Technologies for Asia-Pacific Region* , vol. 4, pp. 1460-1463, 2003.

[7] A. Thanachayanont, "Low voltage CMOS fully differential active inductor and its application to RF bandpass amplifier design," *VLSI Technology, Systems, and Applications, 2001, Proceedings of Technical Papers, International Symposium on*, pp. 125-128, 2001.

[8] Thanachayanont, A. ; Ngow, S.S., "Low voltage high Q VHF CMOS transistor-only active inductor," *Circuits and Systems, The 2002 45th Midwest Symposium on* , vol. 3, pp. 552-555, Aug. 2002.

[9] H. Ugur Uyanik; Nil Tarim, "Compact low voltage high-Q CMOS active inductor suitable for RF applications," *Analog Integrated Circuits and Signal Processing*, vol. 51, no. 3, pp. 191-194, Jun. 2007.

[10] M.M. Reja; I.M. Filanovsky; K. Moez, "Wide Tunable CMOS Active Inductor," Electronics Letters, vol. 44, no. 25, pp. 1461-1463, 12 Dec 2008

Mahdi Ebrahimzadeh (IEEE Student Member 2008) was born in Ardakan, Iran, in 1985. He received the B.S. degree in electronics engineering from Isfahan University of Technology in 2007 and the M.S. degree in electrical engineering from Iran University of Science and Technology, Tehran, in 2010, where he is currently engaged in research toward the Ph.D. degree in electrical engineering.
His present research interests include RF integrated circuits with an emphasis on active inductors and filters, oscillators, frequency synthesizers and high frequency data converters. During 2008-2010 he was with the Electronics Research Center in Iran University of Science and Technology.