PLL Synchronization with PID Controller Based Shunt Active Power Line Conditioners

Karuppanan P and Kamala Kanta Mahapatra

Abstract—This paper describes Shunt Active Power Line Conditioners (APLC) for compensating harmonic currents and reactive power drawn by the non-linear loads besides power factor correction. The shunt APLC is implemented with three phase PWM current controlled voltage source inverter and is connected at the point of common coupling (PCC) for compensating the harmonics. The compensation process is based on phase locked loop (PLL) synchronization with proportional integral derivative (PID) controller. These control strategies for shunt APLC makes certain that source current is sinusoidal even when the load is non-linear and unbalanced. The PWM-VSI inverter switching is done according to gating signals derived from hysteresis band current controller (HCC) and the capacitor voltage is maintained constant using PID controller. The proposed shunt APLC is investigated using extensive simulation and is found to be effective in terms of THD, reactive power compensation and VDC settling time under various balanced and unbalanced load conditions.

Index Terms—Active Power Filter (APF), PLL Synchronization, PID, Hysteresis Current Controller (HCC), Harmonics.

I. INTRODUCTION

Active power line conditioners (APLC) or active power filters (APF) have become significant for solving power quality problems [1-2]. In recent times power quality issue in industrial as well as manufacturing utilities has become a matter of serious concern due to the intensive use of power electronic equipments. Continuing proliferation of nonlinear loads is creating disturbances like harmonic pollution and reactive power problems in the power distribution lines [3-4]. Traditionally these problems are solved by passive filters. But these passive filters introduce tuning problems, resonance, and are large in size and it's also limited to few harmonics [3-4]. So the active power-line conditioners are becomes popular than passive filters; it compensates the current harmonics and reactive power simultaneously.

The APLC can be connected in series or in parallel with the supply network at the point of common coupling (PCC) for compensating harmonic and reactive power. The series active power filter is applicable to voltage harmonic compensation. But most of the industrial applications need current harmonic compensation, so the shunt active filter is popular than series active filter. Shunt APLC attempts to

compensate the current harmonics of the load current by injecting opposite harmonics. The APLC has the ability to keep the mains current balanced and sinusoidal after compensation regardless of whether the load is linear/non-linear and balanced or unbalanced [5-6].

The controller is the heart or primary component of the APF topology. Conventional PI and proportional integral derivative (PID) controllers have been used to estimate the peak reference currents and control the dc side capacitor voltage of the inverter to remain essentially constant. Most of the active filter systems use PI or PID-controller for maintaining the dc side capacitor voltage [7-9]. The phase locked loop (PLL) controller can operate satisfactorily under highly distorted and unbalanced system [3]. However, remarkable progress in the capacity and switching speed of power semiconductor devices such as insulated-gate bipolar transistors (IGBTs), development in the field of microelectronics technology has spurred interest in this area of APLC.

This paper presents proportional integral derivative (PID) with phase locked loop (PLL) synchronization controller based shunt active power filter for the harmonics and reactive power mitigation due to the non-linear and unbalanced loads. The PLL can operate satisfactorily under highly distorted and unbalanced system. The shunt APLC implemented with three phase PWM current controlled voltage source inverter is connected to the ac mains for compensating the current harmonics by injecting equal but opposite current. The reference current(s) for the source are generated using PID controller and PLL controller algorithm. The PWM-VSI gate control signals are brought out from hysteresis band current control technique. The capacitor voltage on the dc side of the inverter is continuously maintained constant with the help of PID controller. The proposed concept for shunt APLC is validated through extensive simulation under both balanced and unbalanced loads conditions.

II. DESIGN OF SHUNT APLC SYSTEM

Shunt APLC is connected to the point of common coupling through filter inductances and operates in a closed loop. The three phase active filter comprises six power transistors with diodes, a dc capacitor, filter inductor and the compensation controller (contains the PLL with PID controller and hysteresis current controller) and is shown in Fig 1. The filter inductor suppresses the higher order harmonics caused by the switching operation of the power transistors. The filter provides smoothing and isolation for high frequency components and the desired current is obtained by accurately controlling the switching of the inverter. Control of the

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current wave shape is limited by switching frequency of inverter and by the available driving voltage across the interfacing inductance [5].

Fig 1 Shunt APLC implemented with PWM-VSI for the distribution system

The three phase source is connected to a diode rectifier (non-linear) load. This nonlinear load current contains fundamental component and higher order of harmonic components. For this system, the instantaneous load current can be written as

$$i_L(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \Phi_n) = I_1 \sin(\omega t + \Phi_1) + \left(\sum_{n=2}^{\infty} I_n \sin(n\omega t + \Phi_n) \right) \quad (1)$$

The load power comprises fundamental power and reactive power including harmonic power. The instantaneous load power can be written as

$$p_L(t) = i_s(t) * v_s(t) = V_m \sin^2 \omega t * \cos \phi_1 + V_m I_1 \sin \omega t * \cos \omega t * \sin \phi_1 + V_m \sin \omega t * \left(\sum_{n=2}^{\infty} I_n \sin(n\omega t + \Phi_n) \right) = p_f(t) + p_r(t) + p_h(t) \quad (2)$$

Here $p_f(t)$ is the fundamental component of power, $p_r(t)$ is the reactive power and $p_h(t)$ represents harmonic power. From this equation the real (fundamental) power drawn by the load is

$$p_f(t) = V_m I_1 \sin^2 \omega t * \cos \phi_1 = v_s(t) * i_s(t) \quad (3)$$

The source current drawn from the mains after compensation should be sinusoidal; this is represented as

$$i_s(t) = p_f(t) / v_s(t) = I_1 \cos \phi_1 \sin \omega t = I_{\max} \sin \omega t \quad (4)$$

If the active power line conditioner provides the total reactive and harmonic power, source current $i_s(t)$ will be in phase with the utility voltage and would be sinusoidal. At this time, the active filter must provide the compensation current:

$$i_c(t) = i_L(t) - i_s(t) \quad (5)$$

APLC estimates the fundamental from the distorted current and compensates for the harmonic and reactive

component.

III. PROPOSED CONTROL SCHEME

The proposed control scheme includes reference current extraction control strategy using PLL synchronization technique with proportional integral derivative controller and PWM VSI with inner current control using hysteresis current modulator.

A) PID Controller:

Fig 2 PID with PLL Controller block diagram

Fig 2 shows the block diagram of the Proportional Integrator Derivative (PID) control scheme of an APLC. The DC side capacitor voltage is sensed and compared with a reference value. The error $e = V_{dc,ref} - V_{dc}$ at the n^{th} sampling instant is used as input for PID controller. The error signal allows only fundamental frequency with the help of low pass filter (LPF). The LPF filter (Butterworth) has a cutoff frequency (fundamental power frequency) set at 50 Hz. The PID controller is used to control the dc side capacitor voltage of the PWM-inverter. The PID controller is a linear combination of the P, I and D controller. Its transfer function can be represented as

$$H(s) = K_P + \frac{K_I}{s} + K_D(s) \quad (6)$$

where, K_P is the proportional constant that determines the dynamic response of the DC-bus voltage control, K_I is the integration constant that determines its settling time and K_D is the derivative of the error representing the trend. The controller is tuned with proper gain parameters [$K_P = 0.7$, $K_I = 23$, $K_D = 0.01$]. The PID controller estimates the magnitude of peak reference current $I_{\max}$ by control the dc side capacitor voltage of the inverter. The peak reference current multiplied with PLL output generates desired reference current.

B) PLL Synchronization:

The PLL circuit tracks continuously the fundamental frequency of the system voltages (V_{sa}, V_{sb}, V_{sc}). The PLL design should allow proper operation under distorted and unbalanced voltage waveform [3] [6].

Fig 3 synchronizing PLL circuit

The PLL-synchronizing circuit shown in Fig 3 determines automatically the system frequency and the inputs are line voltages V_{ab} ($V_{ab} = V_{sa} - V_{sb}$) and V_{cb} ($V_{cb} = V_{sc} - V_{sb}$). The outputs of the PLL synchronizing circuit are i_{a1}, i_{b1}, i_{c1} the three phase currents. This algorithm is based on the instantaneous active three-phase power expression, it's represented as

$$p_{3\phi} = v_a i_a + v_b i_b + v_c i_c \quad (7)$$

The current feedback signals $i_a(\omega t) = \sin(\omega t)$ and $i_c(\omega t) = \sin(\omega t + 2\pi/3)$ is obtained by the PLL circuit and time integral of output ω is obtained from the PI-Controller. It is having unity amplitude and $i_c(\omega t)$ lead to $120^\circ i_a(\omega t)$ these represent a feedback from the frequency ω . The PLL synchronizing circuit can reach a stable point of operation when the input $p_{3\phi}$ of the PI controller has a zero average value ($p_{3\phi} = 0$) and has minimized low-frequency oscillating portions in three phase voltages. Once the circuit is stabilized, the average value of $p_{3\phi}$ is zero and the phase angle of the supply system voltage at fundamental frequency is reached. At this condition, the currents become orthogonal to the fundamental phase voltage component. The PLL synchronizing output currents are defined as

$$i_{a1} = \sin(\omega t - \pi/2) \quad (8)$$

$$i_{b1} = \sin(\omega t - \pi/2 - 2\pi/3) \quad (9)$$

$$i_{c1} = \sin(\omega t - \pi/2 + 2\pi/3) \quad (10)$$

Therefore the PLL output current signals i_{a1}, i_{b1}, i_{c1} and the distorted/unbalanced source voltages V_{sa}, V_{sb}, V_{sc} of the power supply are measured and which are in phase with the fundamental component. The PLL output multiplied with PID controller output I_{max} generates reference current.

C) Hysteresis Current Modulator:

The hysteresis band current control generates the switching pattern the inverter. There are various current control methods proposed for active power filter configurations but in terms of quick current controllability and easy implementation hysteresis current control method has the highest rating among current control methods.

Hysteresis band current control provides robustness, excellent dynamics and fastest control with minimum hardware. The hysteresis current controller is operated independently for each phase. Each phase current-controller is directly generates the switching signal of the phases that is shown in Fig 4.

Fig 4 Diagram of hysteresis current control

In the case of positive input current, if the error current $e(t)$ between the desired reference current $i_{ref}(t)$ and the actual source current $i_{actual}(t)$ exceeds the upper hysteresis band limit ($+h$), the upper switch of the inverter arm is become OFF and the lower switch is become ON. As a result, the current starts to decrease. If the error current $e(t)$ crosses the lower limit of the hysteresis band ($-h$), the lower switch of the inverter arm is become OFF and the upper switch is become ON. As a result, the current gets back into the hysteresis band and the cycle repeats.

$$S = \begin{cases} 0 & \text{if } i_{actual}(t) > i_{ref}(t) + h \\ 1 & \text{if } i_{actual}(t) < i_{ref}(t) - h \end{cases} \quad (11)$$

Here the hysteresis band limit $h=0.5$. The range of the error signal $e(t)$ directly controls the amount of ripple voltage in the output current from the PWM-VSI.

IV. RESULT AND ANALYSIS

The performance of the proposed control strategy is evaluated through simulation using SIMULINK toolbox in the MATLAB. The system is investigated under balanced and unbalanced conditions. The system parameters used are; Line to line source voltage is 440 V; System frequency (f) is 50 Hz; Source impedance of R_s, L_s is $1 \Omega; 0.1 \text{ mH}$ respectively; Filter impedance of R_c, L_c is $1 \Omega; 1 \text{ mH}$ respectively; Diode rectifier R_L, L_L load: $20 \Omega; 200 \text{ mH}$ respectively; Unbalanced three phase R_L, L_L load impedance: $R1 = 10 \Omega, R2 = 50 \Omega, R3 = 90 \Omega$ and 10 mH respectively; DC side capacitance (C_{DC}) is $1200 \mu\text{F}$; Reference voltage ($V_{DC, ref}$) is 400V and Power devices are IGBT with a freewheeling diode in anti parallel.

Non-linear load condition:

The non-linear or non-sinusoidal RL load consists of a six-pulse diode rectifier and is connected with main ac network. The magnitude of RL of the load are 20 ohms and 200 mH respectively and the simulation time is $T=0$ to $T=0.2\text{s}$. The waveform of source current after compensation

is presented in Fig. 5 (a); that clearly indicates the source current is sinusoidal. The six-pulse diode rectifier load current or source current before compensation is shown in Fig 5 (b). The actual reference currents for three-phase are shown in Fig. 5(c); this wave is obtained from our proposed PLL synchronization in conjunction with PID controller. The shunt APLC supplies the compensating current or harmonic current that is shown in Fig. 5(d). These current waveforms are for a particular phase (phase a). Other phases are not shown as they are only phase shifted by 120°

Fig.5 Simulation results for three-phase APLC under Non-linear load condition (a) Source current after APLC, (b) Load currents or source current before compensation, (c)Reference currents by the PID with PLL control algorithm and (d) Compensation current by APLC

Non-linear Load with Unbalanced conditions:

The three phase unbalanced RL load is connected parallel with diode rectifier (non-linear load) in the three phase distribution network. The unbalanced load condition is investigated and simulated without and with active power line conditioners. Unbalanced three phase RL load impedance are $R1=10\ \Omega$, $R2=50\ \Omega$, $R3=90\ \Omega$ and $L=10\ \text{mH}$ respectively and the simulation time is $T=0$ to $T=0.2\text{s}$. The unbalanced RL load current or source current before compensation is shown in 6 (a). The source current after compensation is presented in Fig. 6 (b) that indicates that the current becomes sinusoidal. The shunt APLC supplies the compensating current based on the proposed controller that is shown in Fig. 6(c). We have additionally achieved power factor correction as shown in Fig. 6(d), a-phase voltage and a-phase current are in phase.

Fig.6 Simulation results for APLC under non-linear with Unbalanced load condition (a) RL Load current or Source current before APLC compensation, (b) PLL synchronization output current (c) Source current after APLC (d) Compensation current by APLC and (e) unity power factor waveforms.

DC side capacitor voltage settling time:

The dc side capacitance voltage and its settling time are controlled by PID controller. This controller reduces the ripples to certain level and makes less settling time; these are shown in Fig 7.

Fig 7 the DC side capacitor voltage settling time controlled by PID a) Non-linear ($t=0.23s$) and b) Unbalanced load ($t=0.031s$)

Real and reactive power measurement:

PLL synchronizing with PID controller based compensation improves power quality. The active power and reactive power are calculated by averaging the voltage-current product at the fundamental frequency 50 Hz, shown in Fig 8.

Fig 8 Active and Reactive power after APLC compensation under the (a) Non-linear load ($P=10.8\text{ kW}$, $Q=0.35\text{ VAR}$) (b) Unbalanced load ($P=11.5\text{ kW}$, $Q=0.11\text{ VAR}$)

The phase locked loop with PID controller based APLC system effectively suppresses the harmonics, compensates reactive power and improves power factor. Real power in watts (W) and reactive power in volt-amperes (VAR) are measured under non-linear and non-linear with unbalanced condition and are presented in table 1

TABLE I REAL (P) AND REACTIVE (Q) POWER MEASUREMENT

Load Condition	Real (P) and Reactive (Q) power measurement	
	Without APLC	With APLC

Non-linear	$P=9.09\text{ kW}$ $Q=1.29\text{ VAR}$	$P=10.80\text{ kW}$ $Q=0.35\text{ VAR}$
	$P=10.41\text{ kW}$ $Q=1.22\text{ VAR}$	$P=11.50\text{ kW}$ $Q=0.11\text{ VAR}$

Order of harmonics plotted:

The Fourier analysis of the source current is done to find magnitudes of different harmonic components. PLL synchronization with PID controller based active power filter compensation is suppressing the harmonic currents that are plotted in Fig 9.

Fig 9 Order of harmonics (a) under the Non-linear load condition, the source current without APLC ($THD=26.86\%$), (b) under the Non-linear condition with APLC ($THD=1.49\%$) and (c) under the unbalanced load condition source current with APLC compensation ($THD=3.74\%$)

Total harmonic distortion measured:

The PID controller and PLL synchronizing control based filter makes source current in the supply sinusoidal. The total harmonic distortion is measured using source current waveform. The total harmonic distortion is measured and compared, and presented in Table 2.

Table II. FFT ANALYSIS OF THD

Condition (THD)	Source Current (I_s) without APLC	Source Current (I_s) with APLC
Non-linear load	26.86 %	1.49 %
Non-linear with Unbalanced	22.98 %	3.74 %
Power factor	0.9143	0.9998

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The simulation is conducted for various non-linear and unbalanced load conditions. The PID controller along with PLL controller based active filter makes source current balanced even if the system is unbalanced. Spectral analysis confirms that the active filter brings the THD of the source current to be less than 5% that is in compliance with IEEE-519 standards for harmonics under both balanced/unbalanced conditions.

V. CONCLUSIONS

In this investigation APLC uses PLL synchronizing circuit along with PID controller. It is demonstrated that PID controller maintains the dc side capacitor voltage nearly constant and also settles early even under unbalanced load conditions. This shunt active power line conditioner connected to the ac mains in parallel with the load; compensates the current harmonics and reactive power under unbalanced and non linear load conditions. The reference current(s) are generated using PID controller with PLL synchronizing control algorithm and PWM-VSI gate control signals are generated from hysteresis band current controller. The proposed shunt APLC validated using extensive simulation. The important performance parameters are presented graphically and THD is found to be 1.49 % under balanced load conditions and 3.74 % under unbalanced a load condition that complies with IEEE 519 standards; thus the superior features of the proposed APLC are established.

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