FPGA Based Implementation of Space Vector Modulated Direct Torque Control For Induction Motor Drive

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Abstract— In this paper, a flexible, high computation speed and cost effective field programmable gate array (FPGA) based space vector modulated (SVM) direct torque control for an induction motor is presented. Direct Torque Control (DTC) is known to produce quick and robust response in ac drives. However, during steady state, notable torque, flux and current pulsations occur. They are reflected in speed estimation, speed response, and also in acoustic noise. This paper introduces a new direct torque control (DTC-SVM) for induction motor drive. DTC using space vector modulation is shown to have the low steady state torque ripple, flux ripple and current distortion that is characteristic of space vector modulation and fast transient performance that is characteristics of direct torque control. The above system has been implemented on the Xilinx Spartan 3E FPGA. Simulation and experiment have been performed to prove the feasibility of the proposed strategy.

Index Terms— SVM, DTC, FPGA, Matlab/Simulink

I. INTRODUCTION

In recent years much research has been developed in order to find simpler control schemes for induction motors that meet the most demanding requirements, such as low torque ripple, low harmonic distortion or quick dynamic response. The direct torque control was first introduced by Takahashi in 1986. The principle is based on limit cycle control and it enables both quick torque response and efficiency operation.[1] DTC control of torque and speed of the motor, which is directly based on the electromagnetic state of the motor [2-3]. It has many advantages compare to field oriented control (FOC), such as less machine parameter dependence, simpler implementation and quicker torque response [4]. It only needs to know the stator flux and torque estimations. The configurations of DTC is simpler than the FOC system due to the absence of frame transformer, current controlled inverter and position encoder, which introduces delays and requires mechanical transducer[5]. In [6] Takahashi had proved the flexibility of DTC compared to FOC. However, the disadvantages of DTC are the high torque and flux ripple, and high current distortion that it produces. It also has poor

performance at low speed due to problems with the stator flux estimation.

As an improvement to the classical DTC scheme direct torque control using space vector modulation (DTC-SVM) for an induction motor was first introduced in 1992[7]. The basis of the DTC-SVM scheme is the calculation of the required voltage space vector to compensate the flux and torque errors exactly by using a predictive technique and then its generation using the SVM at each sample period [8-10].

Owing to the rapid progress in Very Large Scale (VLSI) technology, the development of efficient control circuit of an AC motor drive has become a major trend [11-14]. Today, most of the AC drive in use adopts the DSP digital control strategy for motor control. No doubt, this arrangement has the advantages of simpler circuitry software control and flexibility in adaptation to various applications [15-16]. The 16 bit and 32 bit processors designed for electric drive applications have relatively low computational power. However, the recent advancement of ASIC based devices such as field programmable gate array (FPGA) will be able to provide rapid prototyping, high performance signal processing, high precision and flexibility due to their reconfigurable architecture. FPGAs enable hard real time processing and high computing power based on a direct hardware implementation of algorithms and functionalities [17-18]. Hence FPGAs provide an architecture platform for the implementation of drive, motion and activation controller functionalities.

This paper is organized as follows. In section 2, the space vector modulated direct torque control (DTC-SVM) of an induction motor is firstly presented. Then, sector 3 deals with the design of the FPGA- based control architecture. Finally, simulation and experimental results are presented in section 4 in order to verify the validity of developed control system.

II. THEORITICAL BACKGROUND

Applying the usual space vector transformation to a three phase voltage system, a single space vector is defined by

$$V_s = \frac{3}{2} (v_a + av_b + a^2v_c), \quad (1)$$

Where $a = -1/2 + j\sqrt{3}/2$, and v_a , v_b and v_c are stator phase voltages, it is possible to obtain a simple equations set that describe the AC machine dynamic behavior in a stator fixed coordinate system [19]. These equations are

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$$v_s = R_s i_s + \frac{d\psi_s}{dt} \quad (2)$$

$$0 = R_r i_r + \frac{d\psi_r}{dt} - j\omega_m \psi_r \quad (3)$$

$$\psi_s = L_s i_s + L_m i_r \quad (4)$$

$$\psi_r = L_m i_s + L_r i_r, \quad (5)$$

Where R_s and R_r are the stator and rotor resistances, L_s , L_r and L_m are the stator, rotor and mutual inductances and ω_m is the rotor speed. The basic relation between torque and main fluxes is:

$$T_e = \frac{3}{2} p \frac{k_r}{\sigma L_s} \psi_s \times \psi_r \quad (6)$$

$$= \frac{3}{2} p \frac{k_r}{\sigma L_s} |\psi_s| \cdot |\psi_r| \sin(\delta),$$

where δ , known as load angle is the angle between stator and rotor fluxes as shown in Fig.1, p is the number of pole pairs, $k_r = L_m/L_s$, and $\sigma = 1 - L_m^2/(L_s L_r)$. Based on (6) it is clear that it is possible to achieve machine speed and torque control directly by actuating the load angle.

Figure 1 Rotor flux, Reference and Stator Flux Relations

III. FIELD ORIENTED CONTROL AND CLASSIC DIRECT TORQUE CONTROL

A. Field Oriented Control

Field Oriented Control is based on the decomposition of the instantaneous stator current i_s into two orthogonal components in rotor flux oriented components: one proportional to the flux (i_{sx}) and the other proportional to the torque (i_{sy}). Since both current vectors are perpendicular to each other, a decoupled dynamic system is obtained so that both variables can be controlled separately; achieving a similar operation principle as in DC- drives.

Fig.2 illustrates a simplified control diagram of FOC. Both current components are controlled by individual PI controllers, which compute the corresponding stator voltage vector (v_{sx} , v_{sy}) that will generate the desired correction in the current control loop. Then a stator (α , β). Finally the desired stator voltage vector is generated using space vector

modulation.

Figure 2 Field Oriented Control Block Diagram

B. Direct Torque Control

Due to slow rotor flux dynamics, the easiest way to change the load angle is to force a change in the stator flux vector by the application of the appropriate stator voltage vector v_s . Neglecting the effect of the voltage drop on the stator resistance in (2), the stator flux vector is the time integral of the stator voltage vector. For sampling time Δt sufficiently small, (2) can be approximated by (7).

$$\Delta \Psi_s \approx \Delta t \cdot v_s \quad (7)$$

In classic DTC the stator voltage selection is made by hysteresis comparator as shown in Fig.3 with torque and flux magnitude errors as inputs and a predestined gate pulses look-up table that selects the stator voltage vector corresponding to the desired action.

Figure 3 Classic DTC Control Block Diagram

This control strategy leads to changes from full negative torque to full positive causing high torque ripple. As demonstrated in [20], the capability to actuate on torque greatly depends on the emf $\omega_m \Psi_s$. This means that ripple frequency varies with rotor speed obtaining variable switching frequency and a wide spectrum for ripple and stator current.

IV. PROPOSED SPACE VECTOR MODULATED DIRECT TORQUE CONTROL STRATEGY

In the proposed method, the control objective is to select the exact stator voltage vector (v_s) that changes Ψ_s to meet the load angle reference, and so the desired torque while keeping flux amplitude constant. A space vector modulation algorithm is used to apply the required stator voltage vector. It is expected that torque ripple is almost eliminated, while

zero steady state is achieved with switching frequency.

Figure 4 Proposed DTC-SVM Scheme

The presented strategy uses one PI torque regulator, a simple flux calculation block and no rotating coordinate transformation making the control strategy a straightforward application of (6). This is illustrated by the control block diagram of Fig.4. Here torque controller actuates over the load angle δ to meet torque reference tracking. The stator flux calculator block output is given by

$$\psi_s^* = |\psi_s|^* \cos(\delta + \angle\psi_r) + j|\psi_s|^* \sin(\delta + \angle\psi_r), \quad (8)$$

Where $|\psi_s|^*$ is an arbitrary reference value. The use of rotor angle to obtain stator flux reference means that the proposed method is rotor oriented. The use of a rotatory reference frame aligned with rotor flux allows better torque-flux decoupling, leading to faster transient response.

According to the flux calculator output, the stator flux reference signal is compared with the estimated flux obtaining $\Delta\psi_s$, that is needed to follow the torque reference, as it can be seen in Fig.1. This value is divided by Δt to calculate v_s as in (7). The SVM block performs the classical space vector modulation of v_s to obtain the gate drive pulses for the power circuit.

V. DESIGN OF THE FPGA BASED CONTROL ARCHITECTURE

A low cost Xilinx Spartan 3E FPGA, that contains 4,00,000 logical gates and works at 50 MHz (clock period equal to 20ns), was used as target component for the implementation of this controller. The Spartan 3E generic hardware architecture is composed of a matrix of 5,376 slices, which are configurable logic blocks linked to each other by a programmable interconnection network. The Spartan 3E FPGA architecture includes also 16 embedded [18x18] hardware multipliers, 18 Kb internal block RAM memories and enhanced configurable input/output blocks (IOBs). Compared to standard architecture of microprocessors and DSPs, this specificity of FPGAs gives the designer a new degree of freedom since he can build dedicated hardware architectures that match all the requirements in terms of control performances and implementation constraints.

Thus, these dedicated architectures are designed on the basis of a perfect adequation between the control algorithm to be implemented and its final hardware realization, allowing for example to preserve all the potential parallelism of the chosen algorithm.

However, in many cases, the design of FPGA-based controller architectures is rather intuitive and requires from the designer to master several different knowledges (eg, micro-electronics, control, and electrical machine theories). It is particularly true for complex algorithm structures such as the ones found in drive control applications. This naturally leads many control engineers to prefer standard implementations like DSP solution. Thus, in order to make the design of control algorithms more manageable and less intuitive, the designer has to strictly follow a set of steps and rules, which consist of this kind of methodologies are the reusability of the already made designs, the optimization of the consumed resources of the targeted component, the consideration of the control performances, and finally, the reduction of the development time.

This step is crucial when working on complex algorithms. It is aimed to reduce the design cycle that is also called "time to market". It consists of partitioning the whole control algorithm into subparts that are called modules, which are easier to develop and make sense from a functional point of view. This can be done by identification and extraction of several reusable and independent modules such as regulators, modulation functions, estimators, and vector operators according to the divide a large complex design into subparts that are more manageable. Regularity is aimed to maximize the reuse of already designed modules.

However, at the same time, the designer has to also verify that the chosen algorithm-modular partitioning- satisfies the integration criterion. This criterion incorporates the fact that the implementation process is constrained by the hardware resources of the targeted component. However, as it applied separately to each extracted module, the greater the number of extracted modules is, the lower the level of performances in terms of hardware resources consumption. Therefore, if the hardware constraints are not satisfied, the designer has to reduce the number of extracted modules, even if a certain degree of reusability is lost.

As a result, different reusable modules, with different levels of abstraction, can be extracted and added to a specific library of control of electrical systems. Fig.5 shows the hierarchical levels of FPGA architecture. The first or lowest level includes fine grain operators such as registers and arithmetic operators (adders, multipliers, etc.). The second or middle level comprises the modules of the most common used functions in the control of the most common used functions in the control of electrical systems such as

antiwindup PI controller, PWM, (abc-to-dq) transformation, etc. These modules are built using the first level operators. Finally, the whole control algorithms constitute the third or highest hierarchical level of the library. These blocks are developed using both first and second level methods.

Figure 5 Specific Library of Reusable Modules

A. Generation of VHDL code

The detailed steps are shown in the following diagram in Fig.6. The first step is to determine the parameters of the power electronic section and use them to create a model using the PSB blocks. Also the hardware section of the prototyping board like the ADC can be simulated with a mathematical model. In this way, the control algorithm will be simulated as an exact replica of the real system. The next step is the building of the control algorithm with the use of only Xilinx System Generator blocks [21].

Figure 6 Induction Motor Drive Controller Design and Implementation Process

Fig.6 shows the interconnections between the control and the power circuit. The next step is the simulation of the complete system in Simulink and VHDL code generation which is done with the “Xilinx System Generator” block. The process is totally automatic except the choice of the FPGA model required. Normally, the FPGA contains some other functions in addition to the algorithm. Therefore the algorithm must be connected to the remainder of the VHDL

code.

This code is created only once and comes with the prototyping platform. A standard interface or VHDL software can be used to join all these codes. The last step is the synthesis and implementation of the VHDL code. This is done with Xilinx software which requires a few simple steps. After this, a configuration file is obtained permitting programming the FPGA. If some modifications of the system are required, only some steps need to be done again so the process will be much faster.

V. EXPERIMENTAL SETUP

In order to illustrate the efficiency of the proposed FPGA-based space vector modulated direct torque controller, experiments were carried out on a Spartan 3E FPGA-based prototyping platform.

Figure 7 Experimental Setup

The proposed control system is presented in Fig 7. The whole execution time of the space vector modulated direct torque controller is only equal to 3.5 μ s as mentioned previously. As a result, the feedback control is performed quasi instantaneously and the delays in the feedback loop are very small compared to the process time scale.

Thus, by implementing this controller in an FPGA, very good performance is reached. Note that, thanks to the inherent parallelism of FPGA-based solutions and their great flexibility to achieve different control functions. It is also processed with a different sampling frequency equal to 20 KHz.

VI. SIMULATION AND EXPERIMENT RESULT

The space vector modulated direct torque control for induction motor is simulated using Matlab/Simulink [22] and simulated results are shown in Fig.8.

Figure 8 simulation Results of SVPWM

(a) N=200 rpm

(b) N=1000 rpm

Figure 9 Phase Voltage generated by SVPWM Inverter

Fig.9 shows the pulse pattern generated by an FPGA at 200 rpm and 1000 rpm for phase A and Fig.10 shows the voltage generated by SVPWM inverter at different speeds and it can be applied as input for induction motor.

(b) N=1000 rpm

Figure 9 Pulse Pattern Generated by an FPGA

(a) N=200 rpm

VII. CONCLUSION

A full digital controller for space vector modulated direct torque control for induction motor has been proposed. The main advantage of this method is that the all the logic is executed continuously and simultaneously and new high speed algorithms can be used in this way. Implementing the control algorithm in a hardware description language (HDL) allows high flexibility and technology independence. The same algorithm can be directly synthesized into any other FPGA or even in an ASIC.

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