

An Effective Space-Vector PWM Method for Multi-level Inverter Based on Two-level Inverter

P.Satish Kumar, J.Amarnath and S.V.L.Narasimham

Abstract— In this paper, an effective space vector pulse width modulation (SVPWM) method for multi-level inverter fed induction motor is presented. This method is based on SVPWM method for two-level inverter. As the number of level increasing, the SVPWM method becomes more and more complex. An intrinsic relationship between multi-level and two-level is developed and by using a linear transformation, the switching time of vectors for two-level inverter can be transformed for multi-level inverter. A novel classification of voltage vectors is proposed to determine switching sequence. This method can be extended for N-level inverter also. The simulation is carried out up to the nine-level inverter fed induction motor and the results are provided. The results have been good agreement with the published work.

Index Terms— Multi-level inverter, SVPWM, modulation index, induction motor.

I. INTRODUCTION

Multi-level diode clamped voltage fed inverters are recently becoming very popular for multi-megawatt power applications. The main advantage of such an inverter topology is voltage division, i.e., the output voltage is produced through small steps of voltage, and therefore the individual switches are submitted only to these small voltages steps [1]. The other advantages are low harmonic distortion at output, low dv/dt and extended range of under modulation. The multilevel inverters have many advantages than two-level inverters like low harmonic distortion of the ac currents, low switching losses, less blocking voltage of the switching device. But it has the disadvantages like the increased number of switching devices and the complex control algorithm. To control multilevel converters, the pulse width modulation (PWM) strategies are the most effective, especially the space vector pulse width modulation (SVPWM) one, which has equally divided zero voltage vectors describing a lower total harmonic distortion [2].

Several studies apply the SVPWM to the multi-level inverter [3]. These works use a typical SVPWM method, which approximate the output voltage by using the nearest

three output vectors. When the reference vector changes from one region to another, it may induce an output vector abrupt change. In addition we need to calculate the switching sequences and switching time of the state at every change of reference voltage location. Thus the complexity is greatly increasing with increasing the level of the inverter.

Traditionally, three phase voltage is transformed reference voltage vector, the angle and amplitude of reference voltage vector is used to calculate the duration-time of voltage vector. But, as the level is increasing, the control algorithm becomes more and more complex [8].

In this paper an effective SVPWM method for multi-level VSI is proposed based on the intrinsic relation between multi-level and two-level inverter. In this method, the dwelling time of vector calculation is derived from two-level inverter. By using a linear transformation, the dwell time of vectors for two-level VSI can be transformed for multi-level VSI. A novel classification of voltage vectors is proposed to determine switching pattern of PWM sequence and applied for nine-level inverter shown in Fig. 1 and can be extended to n-level inverter also.

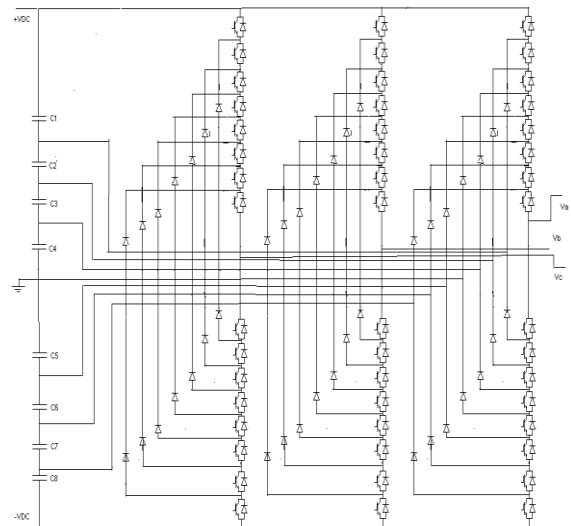


Fig. 1 Nine-level Neutral Point Clamped inverter

II. THE RELATIONSHIP BETWEEN THREE-LEVEL AND TWO-LEVEL INVERTER

In case of nearest three vector (NTV) approach, the first step of SVPWM is to confirm a sub-section that reference vector located in, and the second step is calculation of the dwell time. As the number of level of inverters increasing, the sub-section is very small, so the completion of the algorithm of sub-section

P.Satish Kumar is with the Department of Electrical Engineering, University College of Engineering, Osmania University, Hyderabad, Andhra Pradesh, INDIA-500007, (e-mail: satish_8020@yahoo.co.in).

J.Amarnath is with the Department of Electrical and Electronics Engineering, J.N.T.University Hyderabad, Andhra Pradesh, INDIA (e-mail: amarnathjinka@yahoo.com).

S.V.L.Narasimham is with the School of Information Technology, J.N.T.University, Hyderabad, Andhra Pradesh, INDIA. (e-mail: svlnarasimham@jntuh.ac.in).

is not impossible in one sample period, if traditional SVPWM for multi-level inverters. In this section, a novel SVPWM method for multi-level inverters is proposed.

A. SVPWM algorithm for two-level inverters

The space vector diagram of two-level inverter is as shown in Fig. 2. The reference voltage vector can be defined as

$$V^* = V_A + V_B e^{j\frac{2\pi}{3}} + V_C e^{j\frac{4\pi}{3}} \quad (1)$$

The basic idea of SVPWM is to compensate the required volt-seconds using discrete switching states and their on-times. The equation is

$$\begin{bmatrix} V'_{1x} & V'_{2x} & 0 \\ jV'_{1y} & jV'_{2y} & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} t'_1 \\ t'_2 \\ T \end{bmatrix} = \begin{bmatrix} V_x^* T \\ jV_y^* T \\ T \end{bmatrix} \quad (2)$$

The dwelling time of vector can be calculated as

$$\begin{aligned} t'_1 &= mT \sin\left(\frac{\pi}{3} - \theta\right) \\ t'_2 &= mT \sin(\theta) \\ t'_0 &= T - t'_1 - t'_2 \end{aligned} \quad (3)$$

$m = \sqrt{3} \left(\frac{V_{sr}}{U_d} \right)$ = modulation index, θ is rotation angle of

reference vector, t'_1, t'_2 and t'_0 are dwell time of voltage vector V'_1, V'_2 and V'_0 respectively.

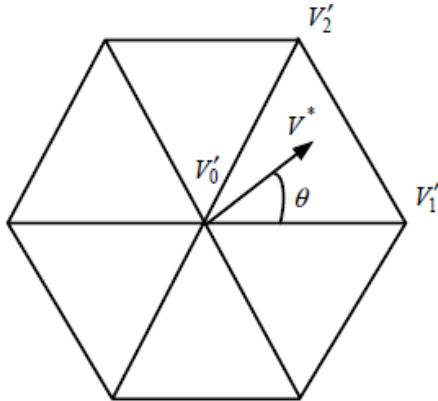


Fig. 2 Space vector diagram of two-level inverter

B. The rule of section determination

The NTV algorithm chooses states exclusively based on their proximity to the reference vector position, disregarding any other criterion, which leads to the lowest ripple at the terminals and the best THD. This approach of choosing the NTVs prevents large steps in the pole-to-pole voltage and if the redundant states are chosen appropriately within a switching period, adjacent state switching can be obtained on all three pole voltages as well, minimizing switching events and losses. The triangle formed by the voltage vectors V_0, V_1 and V_2 . This triangle is divided into four small triangles A1, A2, A3 and A4. In the space voltage vector PWM, generally, output voltage vector is formed by its nearest three vectors in order to minimize the harmonic components of the output voltage and the current. The duration of each vector can be calculated by vector calculation. The three-level inverter can be seen as a two-level inverter of full DC bus.

C. The Space vector dwell time calculation

The space vector diagram for three-level inverter is shown in Fig.3. The dwell time of vector should satisfy the equation

$$\begin{aligned} t_1 V_1 + t_2 V_2 + t_3 V_3 &= V^* T \\ t_1 + t_2 + t_3 &= T \end{aligned} \quad (4)$$

That is

$$\begin{bmatrix} V_{1x} & V_{2x} & V_{3x} \\ jV_{1y} & jV_{2y} & jV_{3y} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} V_x^* T \\ jV_y^* T \\ T \end{bmatrix} \quad (5)$$

The relationship between voltage vector of two-level and three-level is

$$\begin{aligned} V_1 &= a_1 V'_1 + b_1 V'_2 = (a_1 V'_{1x} + b_1 V'_{2x}) + j(a_1 V'_{1y} + b_1 V'_{2y}) \\ V_2 &= a_2 V'_1 + b_2 V'_2 = (a_2 V'_{1x} + b_2 V'_{2x}) + j(a_2 V'_{1y} + b_2 V'_{2y}) \\ V_3 &= a_3 V'_1 + b_3 V'_2 = (a_3 V'_{1x} + b_3 V'_{2x}) + j(a_3 V'_{1y} + b_3 V'_{2y}) \end{aligned} \quad (6)$$

Describe eq. (6) as matrix form, and substitute in eq. (5) it gives

$$\begin{bmatrix} V'_{1x} & V'_{2x} & 0 \\ jV'_{1y} & jV'_{2y} & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} V_x^* T \\ jV_y^* T \\ T \end{bmatrix} \quad (7)$$

Comparing eq. (2) with eq. (7) and considering that the first left matrix is reversible, so the dwell time for three-level inverter can be described as

$$\begin{bmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} = \begin{bmatrix} t_1 \\ t_2 \\ T \end{bmatrix} \quad (8)$$

The matrix in eq. (8) is also reversible, otherwise the nearest three vectors are located on one same line, and it conflict with the basic rule of NTV approach. So the dwell time for three-level inverter can be described as

$$\begin{bmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ 1 & 1 & 1 \end{bmatrix}^{-1} \begin{bmatrix} t'_1 \\ t'_2 \\ T \end{bmatrix} = \begin{bmatrix} t_1 \\ t_2 \\ t_3 \end{bmatrix} \quad (9)$$

By solution eq. (9), the dwell time of vectors for three-level inverter can be acquired. There is a simple linear relationship between dwell time for two-level inverter and three-level inverter. Using a linear transformation, the dwell time of vectors for three-level inverters can be calculated easily. This method can be extended to five or more level inverter simply.

III. CLASSIFICATION OF VOLTAGE VECTOR AND SWITCHING PATTERN GENERATION

A. Three-level Inverter

The switching states of three-level inverter can be classified in to four groups and represented by a space vector diagram as shown in Fig. 3. They can be classified into zero vectors, small vectors (vertices of inner hexagon), medium vectors (mid-points of sides of outer hexagon), and large vectors (vertices of outer hexagon). Both the zero and small vectors have redundant switching states. The DC bus voltage is split into three levels by using two dc capacitors, C_1 and C_2 . Each

capacitor has $V_{dc}/2$ volts and each voltage stress will be limited to one capacitor level through clamping diodes. In case of 3-level NPC inverter, clamping diodes clamped the dc bus voltage into three voltage level, $+V_{dc}/2$, 0 and $-V_{dc}/2$. And there are N^3 possible states i.e., 27 states for three level inverter and it consists of $(3-1)$ capacitors on the DC bus, $2(3-1) = 4$ switching devices per phase and $2(3-2) = 2$ clamping diodes per phase.

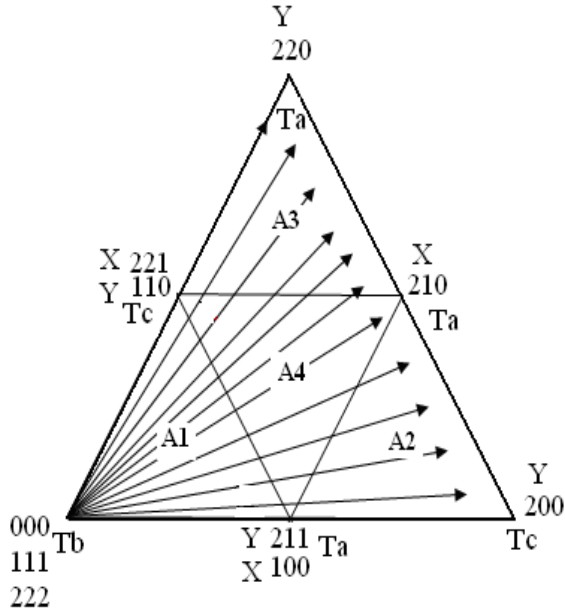


Fig. 3 Space vector diagram of three-level inverter in sextant-I

Space vector diagrams will be chosen for each modulation cycle in order to generate the reference vector (V_{sr}). The vector nearest to V_{sr} are the most appropriate selections in terms of their ability to minimizing the switching frequency of power devices, improve the quality of the output voltage spectra. The space vector diagram of the three-level inverter is divided into six sextants, and each sextant is divided into four triangular regions in order show the vectors nearest to the reference. Three-level inverter consists of large voltage Vectors (LVV), middle voltage Vectors (MVV), lower Small voltage Vectors (LSVV), upper small voltage vectors (USVV) and zero voltage vectors(ZVV) as shown in Table I.

TABLE I: CLASSIFICATION OF VOLTAGE VECTORS

Voltage vector	Symbols
ZVV	(000),(111),(222)
LSVV	(100),(010),(001), (110),(101),(011)
USVV	(211),(121),(112), (221),(212),(112)
MVV	(210),(120),(021), (012),(102),(201)
LVV	(200),(220),(020), (022),(002),(202)

For describing the switching sequence of voltage vectors, a new method to classify vector is introduced in this paper. We divide all voltage vectors into X group and Y group, as shown in Table II. The standard of classification is the present vector that is belongs to group X, if only one level changing in one phase, the next vector belongs to Y. All LVVs belong to group Y, and all MVVs belong to group X. the LSVV and USVV, that locate in same place, are belong to group X and group Y respectively. Such as, 100 is belong to group X, 211 is belong to Y. If the present vector is 010, that belong to group X, it can reach 110, 020, 011 after one switching operation in only one phase, the new voltage vectors belong to group Y all. By using this method of classification, there are two X-group vectors and two Y-group vectors in outer sextant, and three X-group vectors and two Y-group vectors in middle sextant, and four X-group vectors and three Y-group vectors in inner sextant.

TABLE II: CLASSIFICATION OF VOLTAGE VECTORS ACCORDING TO SWITCHING SEQUENCE

X	(111)	(1,00),(010), (001),(221), (212),(122)	(210),(120), (021)(012), (102),(201)
Y	(000),(222)	(110),(101), (011),(211), (121),(112),	(200),(220), (020)(022), (002),(202)

According the criteria proposed in previous section, it can be seen that the output vector always alternate between X-group and Y-group. After odd times varying, vector reach the other group, and even times varying, vector reach the same group.

TABLE III: SWITCHING SEQUENCE

Region	(ON-Sequence)	(OFF- Sequence)
A2	211-210-200-100	100-200-210-211
A3	221-220-210-110	110-210-220-221
A4	211-210-110-100	110-210-211-221

B. Nine-level Inverter

The schematic diagram of nine-level inverter is shown in Fig. 1. The dc bus voltage is split into nine levels by using eight dc capacitors, $C_1, C_2, C_3, C_4, C_5, C_6, C_7$ and C_8 . Each capacitor has $V_{dc}/8$ volts and each voltage stress will be limited to one capacitor level through clamping diodes. In case of nine-level inverter, clamping diodes clamped the dc bus voltage into three voltage level, $+V_{dc}/8, +V_{dc}/8, +V_{dc}/8, +V_{dc}/8, 0, -V_{dc}/8, -V_{dc}/8, -V_{dc}/8, -V_{dc}/8$. And there are N^3 possible states i.e., 729 states for nine-level inverter and it consists of $(9-1)$ capacitors on the DC bus, $2(9-1) = 16$ switching devices per phase and $2(9-2) = 14$ clamping diodes per phase.

The space vector modulation diagram of the nine-level inverter is divided into six sextants, and each sextant is divided into sixty-four triangular regions in order show the

vectors nearest to the reference voltage. Fig. 4 shows the space vector diagram of nine-level inverter in sextant-I.

The voltage vectors of nine-level inverter are divided into X group and Y group, as shown in Table IV. The procedure of selecting the voltage vector of X and Y groups are similar to that of three-level inverter. Table V shows the switching ON sequence and OFF sequence for all the regions of sextant-I of nine-level inverter.

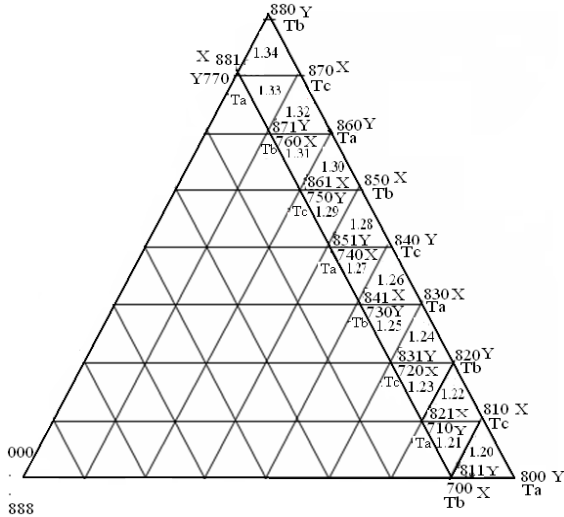


Fig. 4 Space vector diagram of nine-level inverter in sextant-I

TABLE IV: CLASSIFICATION OF VOLTAGE VECTORS ACCORDING TO THEIR SWITCHING SEQUENCE

X	(700)(720)(740)(760)(470)(270)(070)(072)	
	(074)(076)(067)(047)(027)(007)(207)(407)	
	(607)(706)(704)(702)(821)(841)(861)(881)	
	(681)(481)(281)(182)(184)(186)(188)(168)	
	(148)(618)(818)(816)(814)(812)(810)(830)	
	(850)(870)(780)(580)(380)(180)(018)(083)	
	(085)(087)(078)(058)(038)(018)(108)(308)	
	(508)(708)(807)(805)(803)(801)	
	Y	(710)(730)(750)(770)(570)(370)(170)(071)
		(073)(075)(077)(057)(037)(017)(107)(307)
(507)(707)(705)(703)(701)(811)(831)(851)		
(871)(781)(581)(381)(181)(183)(185)(187)		
(178)(817)(815)(813)(800)(820)(840)(860)		
(880)(680)(480)(280)(080)(082)(084)(086)		
(088)(068)(048)(028)(008)(208)(408)(608)		
(808)(806)(804)(802)		

TABLE V: SWITCHING PATTERN

Region	ON-Sequence	OFF-Sequence
1.20	811-810-800-700	700-800-810-811
1.21	811-810-710-700	710-810-811-821

1.22	821-820-810-710	710-810-820-821
1.23	821-820-720-710	720-820-821-831
1.24	831-830-820-720	720-820-830-831
1.25	831-830-730-720	730-830-831-841
1.26	841-840-830-730	730-830-840-841
1.27	841-840-740-730	740-840-841-851
1.28	851-850-840-740	740-840-850-851
1.29	851-850-750-740	750-850-851-861
1.30	861-860-850-750	750-850-860-861
1.31	861-860-760-750	760-860-861-871
1.32	871-870-860-760	760-860-870-871
1.33	871-870-770-760	770-870-871-881
1.34	881-880-871-770	770-871-880-881

IV. ALGORITHM EXTENDED TO N-LEVEL INVERTERS

The SVPWM algorithm for N-level inverter, the first step is to identify triangle that reference vector located in. Then the voltage vectors located on acmes of triangle be used to synthesize the reference vector. As discussion above, we regard N-level inverter is seen as a two level inverter of full DC bus. The dwell times of vectors that be used to synthesize reference vector can be calculated in two-level inverter. For simplifying discussion, we name triangle by a three dimension array, which is defined as

$$\begin{aligned} \lambda_1 &= \text{floor}[t_{1,2} \times (N-1)] \\ \lambda_2 &= \text{floor}[t_{2,2} \times (N-1)] \\ \lambda_0 &= \text{floor}[t_{0,2} \times (N-1)] \end{aligned} \quad (10)$$

Then triangle can be named by a three-dimension array, for example Section $[\lambda_0 \lambda_1 \lambda_2]$. Fig. 5 is space vector diagram of nine-level inverter

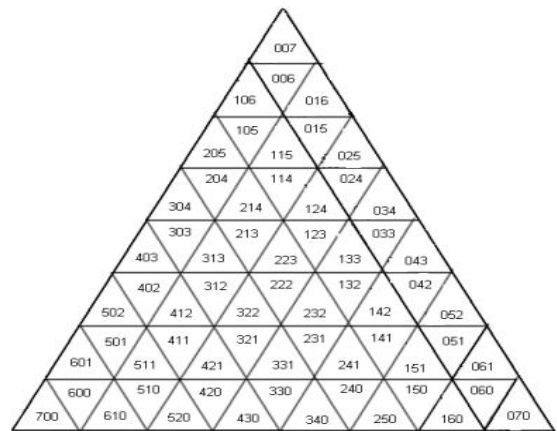


Fig. 5 space vector diagram of nine-level inverter in sextant-I

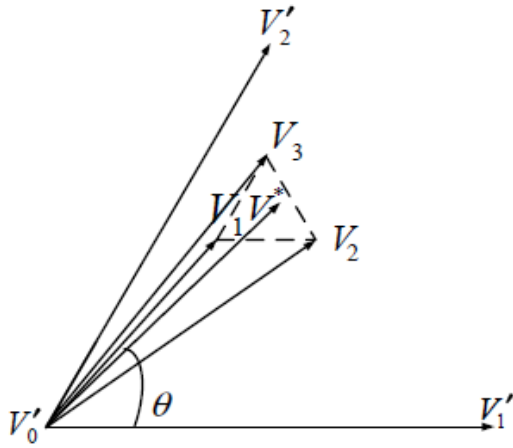


Fig. 6 N-level vector synthesizing relationship deduce by two-level Inverter

We can get the following conclusions:

- 1) There is only one bit is changed between names of adjacent triangles.
- 2) The last bit each row is the same, the similar conclusion of other condition can be acquired easily.
- 3) If reference vector is located on acmes of triangle, we can get $\lambda_1 + \lambda_2 + \lambda_0 = N-1$.
- 4) The 3 bits code's sum of the triangle which has the same direction with the vector's triangle of two-level inverter is concluded as $\lambda_1 + \lambda_2 + \lambda_0 = N-2$.
- 5) The 3 bit code's sum of the triangle which has the opposite direction with the vector's triangle of two-level inverter is concluded as $\lambda_1 + \lambda_2 + \lambda_0 = N-3$.

After identifying the triangle reference vector located in it, we can choose the voltage vector of NTVs to compound reference vector. As shown in Fig.6, according to volt-second balancing principle, the relation of synthesizing of voltage vector to reference vector is:

$$\begin{aligned} t_1 V_1 + t_{2,N} V_{2,N} + t_{3,N} V_{3,N} &= V^* T_s \\ t_{1,N} + t_{2,N} + t_{3,N} &= T_s \end{aligned} \quad (11)$$

That is

$$\begin{bmatrix} V_{1,Nx} & V_{2,Nx} & V_{3,Nx} \\ jV_{1,Ny} & jV_{2,Ny} & jV_{3,Ny} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_{1,N} \\ t_{2,N} \\ t_{3,N} \end{bmatrix} = \begin{bmatrix} V_x^* T_s \\ jV_y^* T_s \\ T_s \end{bmatrix} \quad (12)$$

In N-level there is a mapping relation between the three near vector used to synthesize vector and the two nonzero vector of the two-level, which is:

$$\begin{aligned} V_1 &= a_1 V_{1,2} + b_1 V_{2,2} \\ V_2 &= a_2 V_{1,2} + b_2 V_{2,2} \\ V_3 &= a_3 V_{1,2} + b_3 V_{2,2} \end{aligned} \quad (13)$$

Changing (13) into matrix and put it into (12). In complex plane, we can conclude that:

$$\begin{bmatrix} V_{1,2x} & V_{2,2x} & 0 \\ jV_{1,2y} & jV_{2,2y} & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_{1,N} \\ t_{2,N} \\ t_{3,N} \end{bmatrix} = \begin{bmatrix} V_x^* T_s \\ jV_y^* T_s \\ T_s \end{bmatrix} \quad (14)$$

From two-level to N-level inverter, we define the voltage vector transition matrix is:

$$R = \begin{bmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ 1 & 1 & 1 \end{bmatrix} \quad (15)$$

It's easy to prove that matrix R is reversible. Because of the existing of inverse transformation, the inverse transform matrix R^{-1} is just the transform matrix from two-level vector response time to N-level vector response time.

$$\begin{bmatrix} a_1 & a_2 & a_3 \\ b_1 & b_2 & b_3 \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} t_{1,N} \\ t_{2,N} \\ t_{3,N} \end{bmatrix} = \begin{bmatrix} t_{1,2} \\ t_{2,2} \\ T_s \end{bmatrix} \quad (16)$$

$$T_N = \begin{bmatrix} t_{1,N} \\ t_{2,N} \\ t_{3,N} \end{bmatrix} = R^{-1} \begin{bmatrix} t_{1,2} \\ t_{2,2} \\ T_s \end{bmatrix} = R^{-1} T_2 \quad (17)$$

By solution of the equations above, we can carry out the dwell time of the each vector of the nearest three vectors which is used to synthesizing the reference vector. We can see that there is a simple liner mapping relation between the dwell time of vectors in the N-level inverter and its counterpart in the two level inverter's SVPWM arithmetic. The analysis of N-level inverter's space vector is very helpful for us to understand SVPWM algorithm for N-level inverter and its advantage and disadvantage.

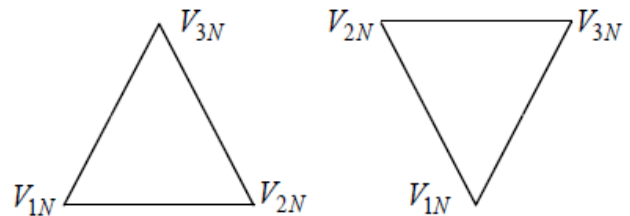


Fig.7 positive and negative triangle in N-level inverter space vector diagram

Any voltage vector of the N-level inverter in a triangle can be expressed as:

$$V = \frac{1}{N} \{ \alpha [100] + \beta [110] + \gamma [111] \}$$

As positive and negative triangle shown in Fig.7, the nearest three vectors have such a relationship:

$$\begin{aligned} V_{1,N} &= \frac{1}{N-1} \{ \lambda_1 [100] + \lambda_2 [110] + \gamma [111] \} \\ V_{2,N} &= \frac{1}{N-1} \{ (\lambda_1 + 1) [100] + \lambda_2 [110] + \gamma [111] \} \\ V_{3,N} &= \frac{1}{N-1} \{ \lambda_1 [100] + (\lambda_2 + 1) [110] + \gamma [111] \} \end{aligned} \quad (18)$$

These two coefficients λ_1 and λ_2 represent the direction and the length of the voltage in N-level inverter, whereas γ is a parameter to control redundancy vector. in positive triangle the voltage vector transform matrix R from two-level to N-level inverter and time transition matrix R^{-1} from two-level

to N-level inverter are, respectively:

$$R_{positive} = \begin{bmatrix} \lambda_1 & \lambda_1+1 & \lambda_1 \\ N-1 & N-1 & N-1 \\ \lambda_2 & \lambda_2 & \lambda_2+1 \\ N-1 & N-1 & N-1 \\ 1 & 1 & 1 \end{bmatrix} \quad (19)$$

$$R_{positive}^{-1} = \begin{bmatrix} -(N-1) & -(N-1) & (\lambda_2+\lambda_1+1) \\ (N-1) & 0 & -\lambda_1 \\ 0 & (N-1) & -\lambda_2 \end{bmatrix} \quad (20)$$

The above matrix is the transition matrix for positive triangle to convert two level control timing to N level control timing. As to negative triangle, we can conclude the vector and the transition matrix are:

$$\begin{aligned} V_{1,N} &= \frac{1}{N-1} \{ \lambda_1 [100] + \lambda_2 [110] + \gamma [111] \} \\ V_{2,N} &= \frac{1}{N-1} \{ (\lambda_1-1) [100] + (\lambda_2+1) [110] + \gamma [111] \} \\ V_{3,N} &= \frac{1}{N-1} \{ \lambda_1 [100] + (\lambda_2+1) [110] + \gamma [111] \} \end{aligned} \quad (21)$$

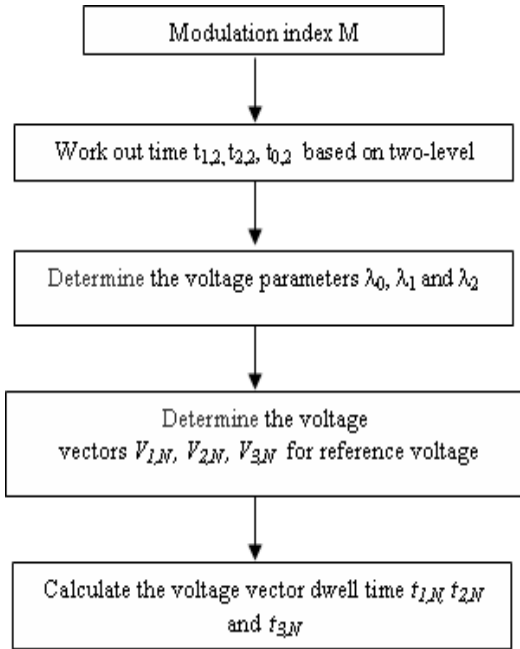


Fig. 8 Flow chart in N-level inverter selection of vector and dwell time

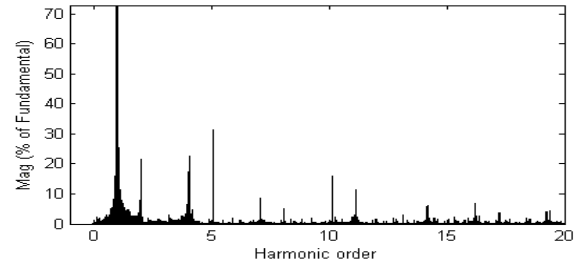
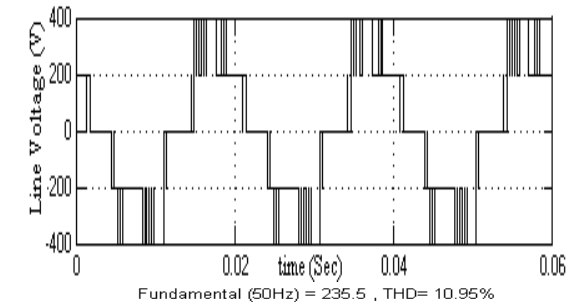
$$R_{negative} = \begin{bmatrix} \lambda_1 & \lambda_1-1 & \lambda_1 \\ N-1 & N-1 & N-1 \\ \lambda_2 & \lambda_2+1 & \lambda_2+1 \\ N-1 & N-1 & N-1 \\ 1 & 1 & 1 \end{bmatrix} \quad (22)$$

$$R_{negative}^{-1} = \begin{bmatrix} 0 & -(N-1) & (\lambda_2+1) \\ -(N-1) & 0 & \lambda_1 \\ (N-1) & (N-1) & -(\lambda_1+\lambda_2) \end{bmatrix} \quad (23)$$

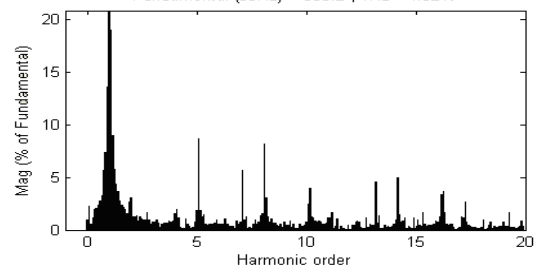
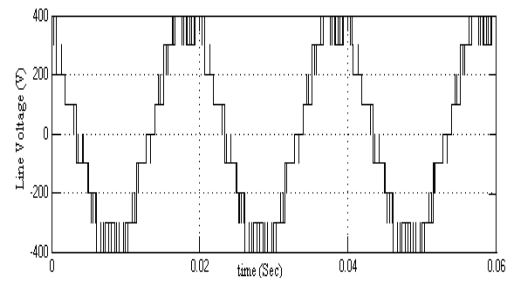
From the analysis it is clear that SVPWM algorithm for any level inverter can be deduced by SVPWM algorithm for two-level. There is a simple transition matrix between them. The flow chart of SVPWM method for N-level inverter is shown in Fig.8.

V. RESULTS AND DISCUSSION

The proposed method is verified by designing a model for N-level inverter and simulated as three-level, five-level, seven-level and nine-level inverter. Fig. 9 shows the line to line voltages and harmonic spectrum of three-level, five-level, seven-level and nine-level inverters. These are entirely the same as traditional SVPWM algorithm and it shows that as the level of inverter is increasing the line voltage is nearly standard sine wave. Fig. 10 shows the stator current, speed and torque of nine-level inverter fed three phase induction motor. Table IV shows the comparison between different levels of inverters. It shows that the THD, rms current and torque ripples are decreasing as the level of inverter increases. In the simulation analysis to the more level, it just modify the level setting number N, therefore it indicate the algorithm is flexible and transplantable.



(a) three-level



(b) five-level

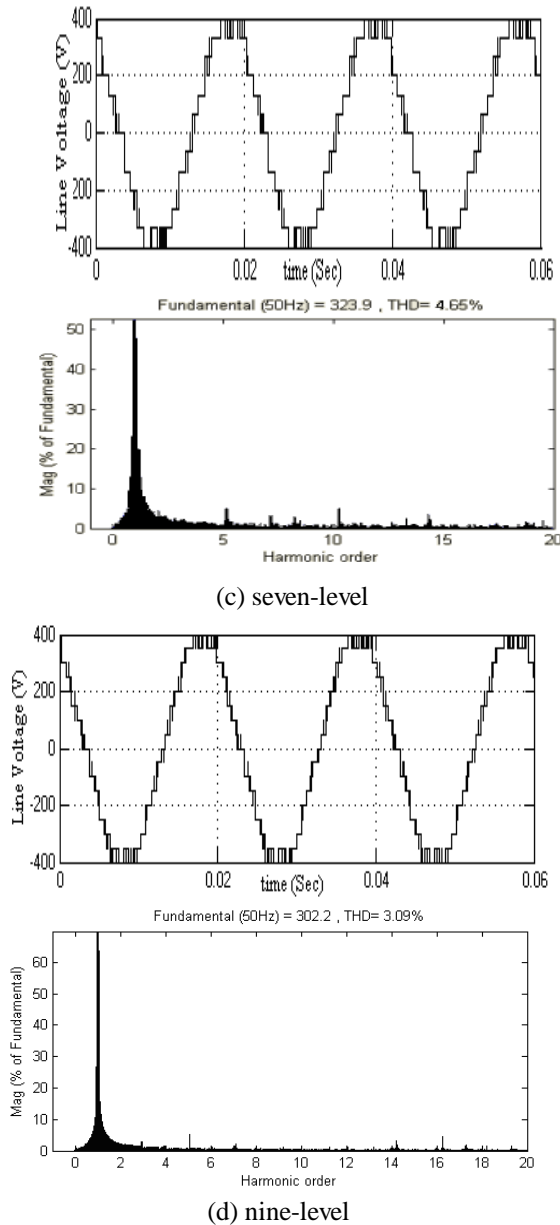


Fig.9 Line to line voltages of Multi-level Inverters and Harmonic analysis

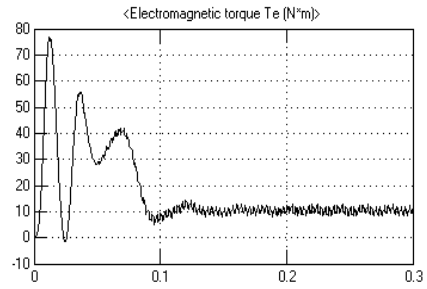
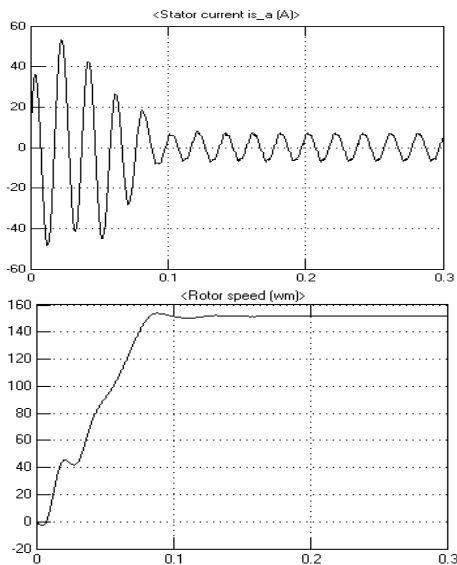


Fig.10 Stator current, speed and torque of nine-level inverter fed induction motor

TABLE IV: COMPARISON BETWEEN MULTI-LEVEL INVERTERS

S.No.	Level of Inverter	THD %	I_{rms} (A)	N rpm	Torque ripple
1	Three-level	10.95 %	6.82	1415	9.2%
2	Five-level	4.82 %	4.86	1440	7.8%
3	Seven-level	4.65 %	4.81	1445	6.5%
4	Nine-level	3.09 %	4.71	1450	4.2%

TABLE V: SIMULATION PARAMETERS

SVPWM Parameters	Modulation index $m = 0.81$
	DC Supply voltage $E = 400V$
	No. of switching intervals $n = 66$
	Switching period $T_s = 300\mu$ sec
Induction Motor Parameters	2 H.P, 4-pole, 400V, 50Hz, 1500rpm, $R_s=1.405\Omega$, $R_r=1.395\Omega$, $L_s=L_r=0.005839H$, $L_m=0.1722H$,

VI. CONCLUSION

In this paper, an effective space vector pulse width modulation (SVPWM) method for multi-level inverter fed induction motor is proposed based on SVPWM method for two-level inverter. An intrinsic relationship between multi-level and two-level is developed and by using a linear transformation, the switching time of vectors for two-level inverter can be transformed for multi-level inverter. A novel classification of voltage vectors is proposed to determine switching sequence. This method can be extended for N-level inverter also. The validity of this method is verified with simulation platform. The simulation is carried out up to the nine-level inverter and verified the results. The results have

been good agreement with the published work.

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P. Satish Kumar was born in Karimnagar, Andhra Pradesh, INDIA in 1974. He obtained the B.Tech degree in electrical engineering from JNTU College of Engineering, Kakinada, A.P., INDIA in 1996 and the M.Tech degree in power electronics from JNTU College of engineering, Hyderabad in 2003. He

worked in various Private Engineering Colleges in Andhra Pradesh for more than eleven years as Associate Professor in the Department of Electrical and Electronics Engineering. Presently he is Senior Assistant Professor in the Department of Electrical Engineering, University College of Engineering, Osmania University, Hyderabad, INDIA. He is presently pursuing Doctoral degree from J.N.T.U. Hyderabad. He presented many research papers in various national and international conferences and journals. His research interests include Power Electronics Drives and Multilevel inverters.



J. Amarnath graduated from Osmania University in the year 1982, M.E from Andhra University in the year 1984 and Ph.D. from J.N.T. University, Hyderabad in the year 2001. He is presently Professor in the Department of Electrical and Electronics Engineering, JNTU College of

Engineering, Hyderabad, India. He presented more than 60 research papers in various national and international conferences and journals. His research areas include Gas Insulated Substations, High Voltage Engineering, Power Systems and Electrical Drives.



S.V.L. Narasimham was born in Bellari, Karnataka State in India in 1961. He received his Bachelors Degree in Electrical and Electronics Engineering in 1982 from JNTU College of Engineering, Jawaharlal Nehru Technological University (JNTU). He obtained his Masters

Degree in Electrical Power Systems in 1987, Masters Degree in Computer Science in 1995 and Ph.D. in 2000 all from JNT University. He joined JNTU as Lecturer in Electrical Engineering in 1991 and is presently professor in Computer Science in School of Information Technology, JNTU. He is guiding many Ph.D. Students and presented more than 50 research papers in various conferences and Journals. He worked as Officer of Special Duty for Andhra Pradesh Transmission Corporation during May 2003 to February 2005. He worked as Senior Manager, e-Projects on Deputation in Centre for Good Governance, a DFID funded AP State Government initiative, during April 2003 to March 2006, where he has exposure to various Government Systems including Power Sector, IT Initiatives and Irrigation. Dr. SVL Narasimham is a Fellow of Institution of Engineers India. His areas of interest are Energy Optimization and Audit, Distribution Systems in Electrical Engineering, Image Processing, Character Recognition, Home Automation and Software Engineering in Computer Science Areas.