International Journal of Computer and Electrical Engineering, Vol. 2, No. 1, February, 2010
1793-8163

Simple Realization of 5-Segment Discontinuous SVPWM Based on FPGA

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***Abstract*—The Space Vector Pulse Width Modulation (SVPWM) is possibly the best among all the PWM techniques for variable frequency drive applications. Unfortunately, the modulation algorithm is mainly implemented with software based on microcontroller or digital signal processors (DSP). These are software-based technique purely and obviously not an ideal solution. Employing Field Programmable Gate Array (FPGA) to realize SVPWM strategies provides advantages that it is considered as an appropriate solution to boost system performance of an SVPWM algorithm. Moreover, although in the literatures the implementation for three-phase SVPWM based on FPGA is not lacking, however all these designs are based on the conventional SVPWM without considering hardware-resource saving and not simple. This paper present a simple realization of 5-segment discontinuous SVPWM with a difference approach based on FPGA, in which the judging of sectors and the calculation of the firing time to generate the SVPWM waveform is simple, and also the switching losses is low. The proposed discontinuous SVPWM has been designed and successfully implemented by using APEX20KE Altera FPGA considering hardware-resource saving and has successfully driven a three phase inverter system with induction machine 1.5 kW as load.**

***Index Terms*—space vector, pulse width modulation, discontinuous SVPWM, FPGA, simple realization**

I. Introduction

The Space Vector Pulse Width Modulation (SVPWM) method is an advanced PWM method and it is possibly the best among all the PWM techniques for variable frequency drive applications. In recent years, this method gradually obtains widespread applications in the power electronics and the electrical drives, because of its superior performance characteristics. Compared to the Sinusoidal Pulse Width Modulation (SPWM), SVPWM is more suitable for digital implementation and can increase the obtainable DC voltage utilization ratio very much. Moreover, it can obtain a better voltage total harmonic distortion factor [1-4]. Up to now, its theories and algorithms have been well developed and applied more widely with the progress of power electronics.

Manuscript received July 13, 2009.

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In most engineering practice, the SVPWM algorithm is mainly implemented with software based on microcontroller or digital signal processors (DSP) are widely adopted. They perform control procedure sequentially by exploiting their mathematically oriented resources. That is the instructions of different procedures are executed one after the other. Thus, the purely software-based technique is not an ideal solution. Employing Field Programmable Gate Array (FPGA) to realize SVPWM strategies provides advantages such as rapid prototyping, simpler hardware and software design, and higher switching frequency. Differ from software implementation; FPGA performs the entire procedures with concurrent operation (parallel processing by means of hardware mode and not occupying) by using its reconfigurable hardware. For its powerful computation ability and flexibility, an FPGA is considered as an appropriate solution to boost system performance of a digital controller including an SVPWM algorithm [2, 5-8].

However, this conventional SVPWM suffers from the drawbacks like computational burden, inferior performance at high modulation indices and high switching losses of the inverter. Hence to reduce the switching losses and to improve the performance in high modulation region, several discontinuous SVPWM methods have been proposed [9-11].

Although in the literatures the implementation for three-phase conventional SVPWM and discontinuous SVPWM based on FPGA is not lacking, however all these designs are based on the conventional SVPWM without considering hardware-resource saving. In this paper, we design and implement a FPGA based SVPWM with a difference approach, in which the judging of sectors and the calculation of the firing time to generate the SVPWM waveform is simple, and also the switching losses is low. In this paper, a novel 5-segment discontinuous SVPWM design based on the basic idea from [4] and [12] is proposed. This scheme is hoped that it has lower switching losses, simpler algorithm and can be implemented easily based on APEX20KE Altera FPGA.

II. The Principles Of Conventional Svpwm

The main aim of any modulation technique is to obtain variable output having a maximum fundamental component with minimum harmonics and less switching losses. The SVPWM technique is more popular than conventional technique. This technique was originally developed as a vector approach to pulse width modulation (PWM) for three phase inverter [1]. It is a more sophisticated technique for generating sinusoidal wave that provides a higher voltage to

the motor with lower total harmonic distortion. It confines space vector to be applied according to the region where the output voltage vector is located.

SVPWM refers to special switching scheme of the six power transistor of a three phase power converter. It is based on fact that there are only two independent variables in a 3-phase voltage system. We can use orthogonal coordinates to represent the 3-phase voltage in the phasor diagram. A three-phase-voltage vector can be expressed as:

$$\mathbf{V}_{\text{ref}} = \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} v_{A0} \\ v_{B0} \\ v_{C0} \end{bmatrix} \quad (1)$$

In the SVPWM scheme, the 3-phase output voltage is represented by a reference vector which rotates at an angular speed of $\omega = 2\pi f$. The task of SVM is to use the combinations of switching states to approximate the reference vector, $\mathbf{V}_{\text{ref}}$. To approximate the locus of $\mathbf{V}_{\text{ref}}$, the eight possible switching states of the inverter are represented as 2 null vectors and 6 active vectors. The operating states and corresponding vectors are listed in Table I.

TABLE I: SWITCHING STATE OF THE 2-LEVEL INVERTER

Space vector		Switching state	On switches **S**
Zero vector	$\mathbf{V}_{\_}$	111	1, 3, 5
	$\mathbf{V}$	000	2, 4, 6
Active vector	$\mathbf{V}$	100	1, 2, 4
	$\mathbf{V}_{\_}$	110	1, 3, 6
	$\mathbf{V}_{\_}$	010	2, 3, 6
	$\mathbf{V}$	011	2, 3, 5
	$\mathbf{V}$	001	2, 4, 5
	$\mathbf{V}_{\_}$	101	1, 4, 5

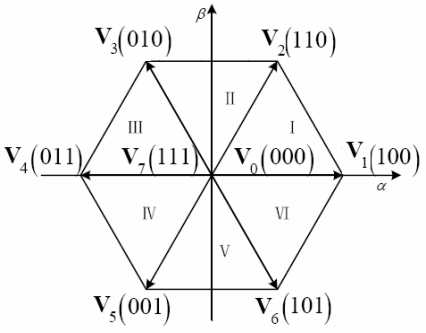
These vectors ($\mathbf{V}_1 \sim \mathbf{V}_6$) can be used to frame the vector plane, which is illustrated in Figure1. The rotating reference vector can be approximated in each switching cycle by switching between the two adjacent active vectors and the zero vectors. In order to maintain the effective switching frequency at a minimal value, the sequence of the toggling between these vectors is organized in such way that only one leg is affected in every step.

A. *Identification of the sector*

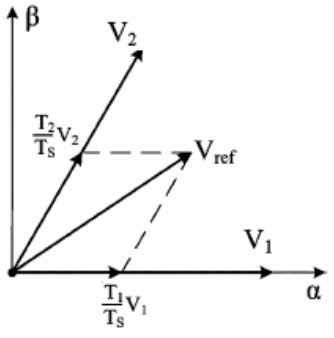
The sector judgment and application time of active vector for all SVM strategies are the same. Based on Figure 1 (a), it is obvious that the sector number is determined by the angle of the reference vector. The identification of k can be generally in αβ coordinates deal with by the appropriate boundary condition according to Table II.

B. *Determination of the duration of active vectors*

For digital control application, the reference inputs are sampled in a regular sampling interval to determine the switching duration of the active vectors. That it, any reference vector inside the hexagon can be obtained two adjacent active vector ($\mathbf{V}_k$,$\mathbf{V}_{k+1}$). Then, $\mathbf{V}_{\text{ref}}$ can be expressed as functions of $\mathbf{V}_k$ and $\mathbf{V}_{k+1}$ by the following equation:



(a)



(b)

Fig. 1 Vector plane frame; (a) space voltage vectors, (b) Decomposition $\mathbf{V}_{\text{ref}}$ with $\mathbf{V}_k$ and $\mathbf{V}_{k+1}$ (e.g., in sector I)

TABLE II: CRITERION OF THE SECTOR IDENTIFICATION IN REF [6]

Sector	Vector Angle	V_α, V_β conditions
I	$(0^0, 60^0)$	$0 \le V_\beta \le \sqrt{3}V_\alpha$
II	$(60^0, 120^0)$	$V_\beta \ge \sqrt{3}V_\alpha$ and $V_\alpha \ge 0$, or $V_\beta \ge -\sqrt{3}V_\alpha$ and $V_\alpha < 0$
III	$(120^0, 180^0)$	$0 \le V_\beta \le -\sqrt{3}V_\alpha$
IV	$(180^0, 240^0)$	$\sqrt{3}V_\alpha < V_\beta \le 0$
V	$(240^0, 300^0)$	$V_\beta \ge \sqrt{3}V_\alpha$ and $V_\alpha \ge 0$, or $V_\beta \ge -\sqrt{3}V_\alpha$ and $V_\alpha < 0$
VI	$(300^0, 360^0)$	$-\sqrt{3}V_\alpha \le V_\beta < 0$

$$V_{ref} = \frac{T_k}{T}V_k + \frac{T_{k+1}}{T}V_{k+1} \quad (2)$$

Where $\mathbf{T}_k$ and $\mathbf{T}_{k+1}$ are the dwell time of $\mathbf{V}_k$ and $\mathbf{V}_{k+1}$ during each sampling period (**T**) each sampling period, respectively, and k is the sector number corresponding to the reference location. For example in sector I, k=1, vector $\mathbf{V}_1$ activates lasting for $\mathbf{T}_1$, and $\mathbf{V}_2$ activates lasting for $\mathbf{T}_2$ during **T**. The principle is similar in all sector of the six sectors, therefore Figure 1 (b) highlights the relation for sector I only.

Considering that magnitude of non zero space satisfies $\|\mathbf{V}_k\| = 2\mathbf{V}_{dc}/3$, the dwelling time can be evaluated by the

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following equations:

$$\begin{cases} T_k = \dfrac{\sqrt{3}}{V_{dc}} T\left(\sin(\dfrac{\pi}{3}k)V_\alpha - \cos(\dfrac{\pi}{3}k)V_\beta \right) \\ T_{k+1} = \dfrac{\sqrt{3}}{V_{dc}} T\left(-\sin(\dfrac{\pi}{3}(k-1))V_\alpha + \cos(\dfrac{\pi}{3}(k-1))V_\beta \right) \\ T_0 = T - T_k - T_{k+1} \end{cases} \quad (3)$$

Where $\mathbf{V}_{dc}$ is the dc-link voltage of the inverter, and $\mathbf{T}_0$ is the switching duration of a zero vector in each sampling period. Suppose the reference is keeping a circular trajectory, the $\mathbf{T}_0$ >0, the output voltage is a regular sinusoidal in linear modulation. As (3), it is theoretically simple but it is obvious that this algorithm required complicated computations with trigonometric function.

C. Switching sequence (switching pattern)

This SVPWM strategy aims to minimize harmonic distortion in the current by selecting the appropriate switching vectors and determining of their corresponding dwelling widths. The flux produced by the reference voltage vector in a SVPWM switching period is a combination of each individual flux resulted by corresponding voltage vector. There are many switching pattern to implementation SVPWM. The choice of the null vector determines the SVPWM scheme. There are a few options: the null vector V_0 only, the null vector V_7 only, or a combination of the null vectors.

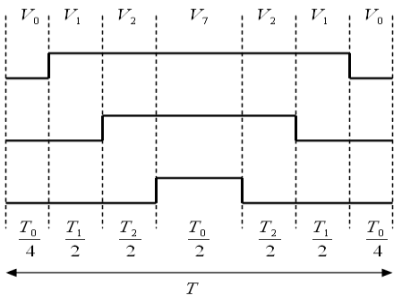

Fig. 2 SVPWM Pattern I (conventional 7-segment switching sequence) of the sector I

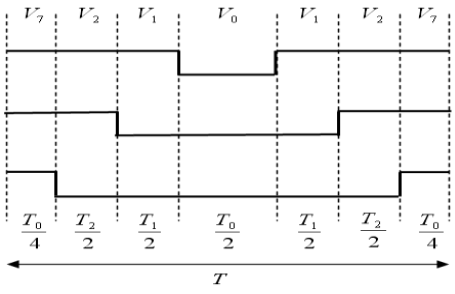

Fig. 3 SVPWM Pattern II (other conventional 7-segment switching sequence) of the sector I

The equivalent PWM waveforms, which produce the same average flux, may consist of various combinations of the basic vectors. However, the sector judgment and application time of active vector for all SVM strategies are the same. Based on [5, 11-13] can be created some switching patterns. Figure 2 and 3 show two different 7-segment algorithm switching sequence patterns of the sector I, while Figure 4 Figure 5 show two different 5-segment algorithm switching sequence patterns of the sector I. Only null vector V_7 and null vector V_0 is used in each cycle respectively. Its sequences are symmetrical too. This scheme lowers the switching times than pattern I. Moreover, the algorithm can be implemented easily by DSP or FPGA.

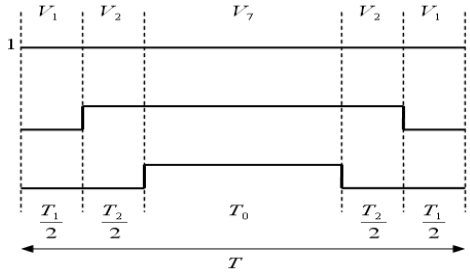

Fig.4 SVPWM Pattern III (5-segment switching sequence) of the sector I

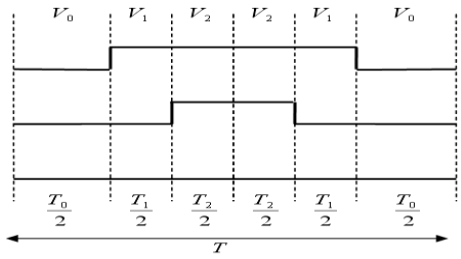

Fig. 5 SVPWM switching Pattern IV (other 5-segment switching sequence) of the sector I

III. A SIMPLE REALIZATION METHOD OF SVPWM ALGORITHM

Different from the conventional principle of SVPWM algorithm, this section will present symmetrical 5-segment discontinuous switching sequence to replace symmetrical 7-segment continuous switching sequence in conventional SVPWM, new judge method of sectors, and new SVPWM generating method based on calculation of the duration of active vectors.

A. Proposed SVPWM switching Pattern (5-segment discontinuous switching sequence)

There has been reported many discontinuous SVPWM pattern [5, 9-11, 13]. However, not all those patterns have lower switching losses, simpler algorithm and can be implemented based on FPGA easily. In this paper, a novel symmetric 5-segment discontinuous SVPWM design refer to the basic idea from [4] and [12] is proposed. This pattern has been successfully implemented based on DSP by Yu [12]. It is known has lower switching losses, simpler algorithm and can be implemented easily. Therefore, this paper proposes to implement this pattern based on FPGA in order to boost system performance of SVPWM. In this pattern, there is always a channel staying constant for the entire PWM period. The state sequence in this pattern is X-Y-Z-Y-X, where Z=1 in sector I, III and V, and Z=0 in the remaining sector. So the number of switching time for this pattern is less than the conventional pattern. The obvious result of this is reduced

switching losses.

B. Proposed identification of the sector

There are many kinds of methods to judge the sector that the reference space voltage vector lies in. Zhi-pu [14] compares the reference space vector's angle with 0^0, 60^0, 120^0, 180^0, 240^0, and 300^0 to obtain the number of the sector that the V_{ref} in. In other references, Yu [15], Jiang [7] and Xing [16] obtain the sector number by analyzing the relationship between V_α and V_β. To determine the sector, they calculate the projections V_a, V_b and V_c of V_α and V_β in (a,b,c) plane by using inverse Clark transformation, as follow:

$$\begin{cases} V_a = V_\beta \\ V_b = \dfrac{\sqrt{3}V_\alpha - V_\beta}{2} \\ V_c = \dfrac{-\sqrt{3}V_\alpha - V_\beta}{2} \end{cases} \quad (4)$$

Then, based on equation (), they calculate N=sign(Va) + 2*sign(Vb) + 4*sign(Vc). Map N to the actual sector of the output voltage reference by referring to Table III.

TABLE III: MAP N TO THE ACTUAL SECTOR OF THE OUTPUT VOLTAGE REFERENCE

N	1	2	3	4	5	6
sector	2	6	1	4	3	5

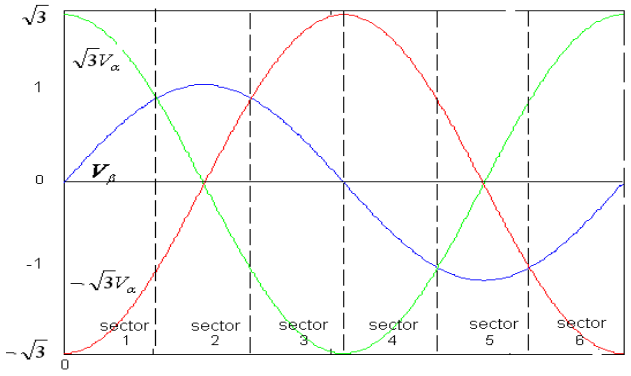

Fig.6 The plotting of $V_\beta, \sqrt{3}V_\alpha, -\sqrt{3}V_\alpha$ wave

TABLE IV: THE PROPOSED IDENTIFICATION OF THE SECTORS

Sector	Vector Angle	$V_\beta > 0$	$V_\beta > \sqrt{3}V_\alpha$	$V_\beta > -\sqrt{3}V_\alpha$
I	$(0^0, 60^0)$	1	0	1
II	$(60^0, 120^0)$	1	1	1
III	$(120^0, 180^0)$	1	1	0
IV	$(180^0, 240^0)$	0	1	0
V	$(240^0, 300^0)$	0	0	0
VI	$(300^0, 360^0)$	0	0	1

1: satisfy, 0: not satisfy

In [17], Zeliang has adopted the new intermediate vector X_α and X_β that it define as $X_\alpha = \frac{3}{2}V_\alpha$ and $X_\beta = \sqrt{3}V_\beta$ as decompose the conventional SVPWM, which will properly counteract the redundant calculations to identify sector location, but it imported the complicated matrix calculations. In this paper, based on analyzing the principle of SVPWM in [7, 15-17] and to reduce burden of computation, a new method to determine the sectors of voltage vectors based on comparison between $V_\beta, \sqrt{3}V_\alpha, -\sqrt{3}V_\alpha$ and 0 as shown in Figure 6 is proposed. Through the comparison, we can determine the sectors of voltage vectors as shown in Table IV.

C. Determination of the duration of active vectors

The space vector technique allows to synthesizing a desired vector V_{ref} from two adjacent actives, V_α and V_β (among V_1 and V_2, as shown in Figure 1) during time interval, T_a and T_b. The null vectors (V_0 and V_7) are also applied to reduce the inverter switching frequency. In the proposed design, only one null vector is inserted in a PWM period, only V_7 for odd sector and only V_0 for even sector.

$$V_{ref} = V_\alpha + jV_\beta = \frac{2T_a}{T}V_\alpha + \frac{2T_b}{T} \quad (5)$$

$$\frac{T}{2} = T_a + T_b + T_0 \quad (6)$$

Hence, the half PWM period T is composed by the switching time T_a, T_b and T_0. The total time of the null vectors can be expressed as

$$T_0 = \frac{T}{2} - T_a - T_b \quad (7)$$

TABLE V: THE SWITCHING TIME OF THE ACTIVE VECTOR FOR EACH SECTOR

Sector	T_a	T_b	$T_a + T_b$
I	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} + \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$
II	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} + \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} + \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$
III	$\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} + \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$
IV	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} + \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$-\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$
V	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$-\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$
VI	$-\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$

In this design, the switching time of the active vectors for each sector can be calculated as shown in Table V.

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D. Proposed SVPWM switching sequence generating method based on calculation of the duration of active vectors

In this paper, with refer to equation $y = \frac{2m}{T}x$ in Figure 7, the PWM generating for odd sector are realized through comparison between triangle and T_a, and between triangle and $T_a + T_b$ with other switching is set equal to 1; while for even sector, the PWM generating are realized through complement of comparison between triangle and T_a, and complement of comparison between triangle and $T_a + T_b$ with other switching is set equal to 0. For example, in sector I if x=T_a= $\frac{T_0}{2}$ then $y = \frac{2m}{T}(\frac{T_0}{2})$ and if x=T_b= $\frac{T_1}{2}$ then $y = \frac{2m}{T}(\frac{T_1}{2})$.

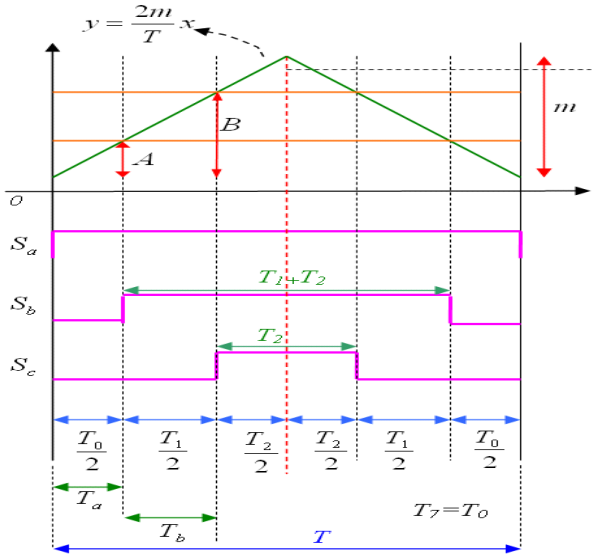

Fig.7 Proposed SVPWM switching sequence generating method

For more simplicity of circuit design, in this paper the term $\frac{2m}{T}$ is set equal to 1, so if x= $\frac{T_0}{2}$ =T_a then y= $\frac{T_0}{2}$ =T_a, and if x= $\frac{T_1}{2}$ then y= $\frac{T_1}{2} = T_b$. Obviously if x= $\frac{T_0}{2} + \frac{T_1}{2} = T_a + T_b$ then y= $\frac{T_0}{2} + \frac{T_1}{2} = T_a + T_b$. Therefore, the PWM generating for S_b and S_c channels in sector I can be obtained through comparison between triangle and T_a, and between triangle and $T_a + T_b$ respectively and S_a Channel is set equal to 1. Moreover, the PWM generating in other sectors can be obtained in the similar way.

IV. FPGA Implementation of A Proposed Novel SVPWM

In previous section, the principle of SVPWM is analyzed. In this section FPGA implementation of a proposed novel SVPWM will be presented. Overall of the proposed SVPWM design is shown in Figure 8. This top module can be sub divided into 5 sub modules, namely *ajust_freq*, *Vbeta_Valfa*, *find_sector*, *SVM_generator* and *deadtime_sytem module*.

A. Adjust of Carrier and Fundamental Frequency Module

In this module, the main clock frequency is designed to connect L6 pin at APEX20KE Altera FPGA board system. It is 33.33 MHz dedicated clock generator in this board. The clocking system to adjust carrier and fundamental frequency is done in this module. In this research, carrier frequency is set to 20 kHz and in temporary, fundamental frequency is set fixed to 50 Hz. It to get carrier and fundamental frequency is done through clock dividing.

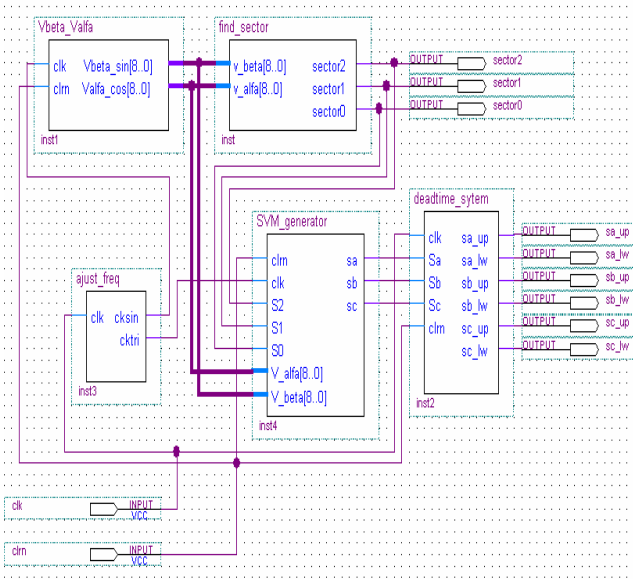

Fig.8 Overall of the proposed SVPWM design

For example, because of the triangle signal generator design in this research is sampled 32 times per period, then it to get 20 kHz is done through dividing of the main clock generator above with 13 (33.33MHz:(13x32)=20 kHz). The fundamental frequency also can be gotten through similar dividing.

B. V_α and V_β Module

In this research, V_α and V_β is generated using sine and cosine function through look up table (LUT) with memory mapping 360 addresses. The lower, base, and higher number of sine and cosine function is represented with 96, 224 and 352 respectively in 9 unsigned bits. The design of V_α and V_β module is shown in Figure 9. Because in this design it uses memory mapping 360 addresses, then the counter mod-360 is used to count LUT of V_α and V_β.

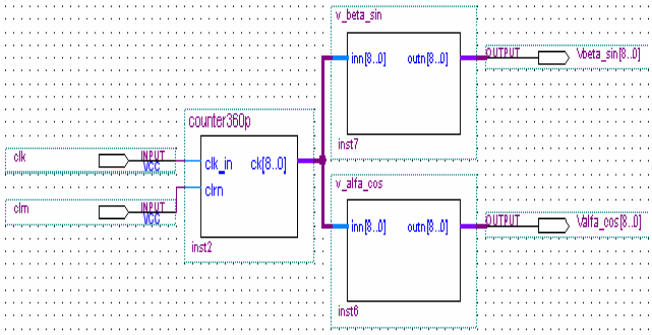

Fig.9 V_α and V_β Module

C. Sector Finder Module

Due to existing different switching time equations, the reference voltage sector knowledge is necessary. The SF module is responsible judging the reference vector sector and does it using Table 2 above. As Figure 10, the "*x_pos_akar*" and "*x_neg_akar*" module are used to multiply between V_α with $\sqrt{3}$ and V_α with $-\sqrt{3}$ respectively. Then, these results of operation are compared with V_β through "*comp9a*" module that it is written is VHDL code, and in other hand V_β is compared with zero through "*compa*" module. It to determine number of sector is done with simplification of truth table that it is developed from the results of comparison above, as shown in Table VI through "*csector*" module.

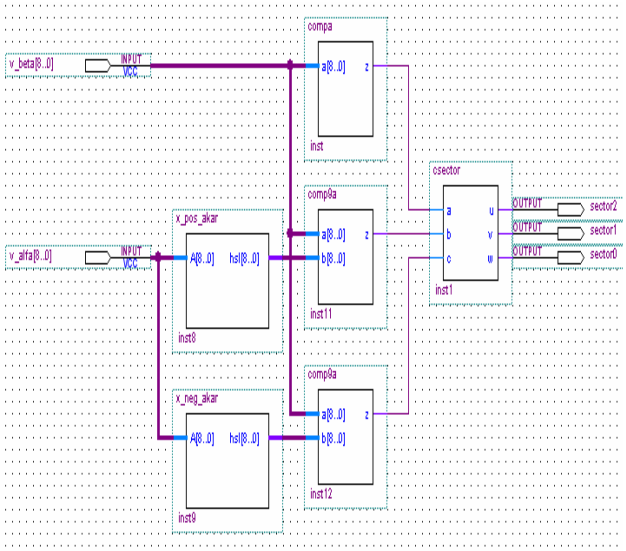

Fig.10 Sector finder (SF) module

TABLE VI: CONVERSION OF RESULT OF COMPARISON BETWEEN $V_\beta, \sqrt{3}V_\alpha, -\sqrt{3}V_\alpha$ AND 0 TO DETERMINE SECTOR

Sector	Vector Angle	**Input**	**Ouput ($S_2S_1S_0$)**
I	(0^0, 60^0)	101	001
II	(60^0, 120^0)	111	010
III	(120^0, 180^0)	110	011
IV	(180^0, 240^0)	010	100
V	(240^0, 300^0)	000	101
VI	(300^0, 360^0)	001	110

D. Three phase SVPWM signal generator module

The overall of three phase SVPWM signal generator module is shown in Figure 11. This module can be sub divided into 4 sub modules, namely *Triangle*, *Duration_Ta*, *Duration_TaTb*, and *SVM pattern* module. *Triangle* module is functioned as triangle signal generator. In this research, one period of triangle signal generator is sampled 32 times, and then it is represented in the digital number 9 unsigned bit, with lower (in this case is same with base number) and higher number each are 224 and 352 respectively. Due to *Duration_Ta* and *Duration_TaTb* module, these modules are digital solution of each second and fourth column respectively. And SVM pattern module as the last module is functioned as SVPWM switching sequence generating as it is described in section 3.4 and it is illustrated in Figure 7.

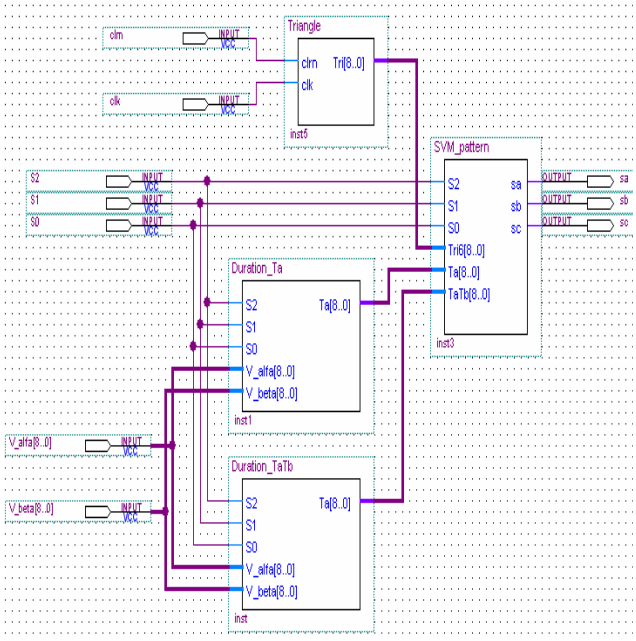

Fig.11 Three phase SVPWM signal generator module

V. Results and Discussions

A. Simulation

This mode is based on the Quartus II, the parameters are listed as follows: V_{dc}/T=1, switching frequency has been tried at 2.5 and 20 kHz, and fundamental frequency 50 Hz. The compilation report of proposed SVPWM generator design is shown in Figure 12 (a), and it more detail for each module in Figure 12 (b). It can be seen that the design requires 520 logic elements and 9.216 memory bits.

Figure 13 show simulation results of the proposed SVPWM generator. These results verify by simulation that the proposed design runs with the desired.

B. Experimental

In previous section it has been shown that the proposed SVPWM generator has worked properly in simulation mode. Therefore, the design can be continued to hardware

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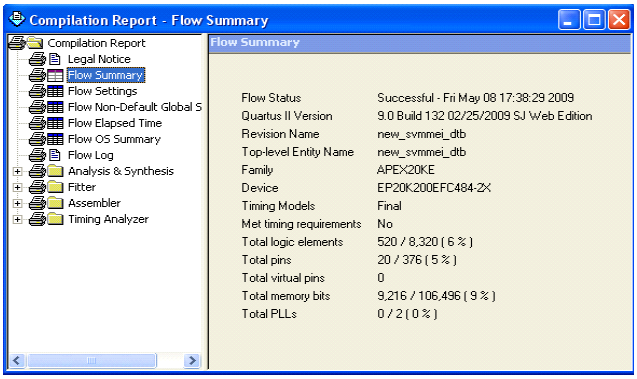
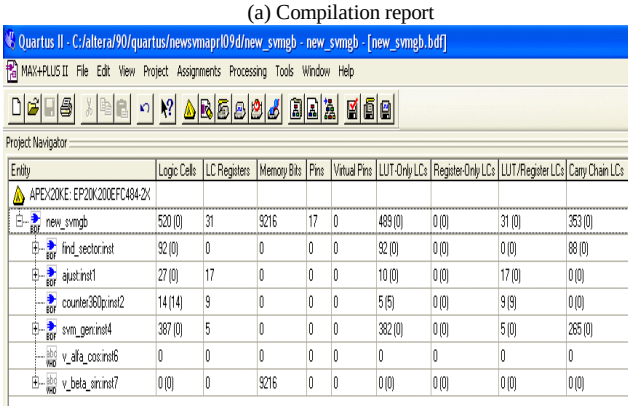
implementation based on FPGA (programmer level). In this research, the proposed SVPWM generator design with some carrier frequency has programmed to APEX20KE Altera FPGA successfully.

The sequence of switching state in each sector and the dead time with 2 μs that they also has been done successfully as shown in Figure 14 and 15 respectively. Inherently, Figure 16 shows hardware implementation of proposed SVPWM generator at carrier frequency 20 kHz. The first, second and third channel at Figure 16 (a) and (b) is each S_a, S_b, and S_c switching state respectively, otherwise fourth channel is each (S_a-S_b) line-to-line switching state and its frequency spectrum respectively. The harmonics due to the 20 kHz switching frequency are clearly visible in Figure 16 (b). The results above have proved that the proposed SVPWM generator has realized in hardware platform based on FPGA and has run with desired.



(a) Compilation report



(b) The using of FPGA resource in detail

Fig.12 The using of FPGA resource of proposed SVPWM generator design

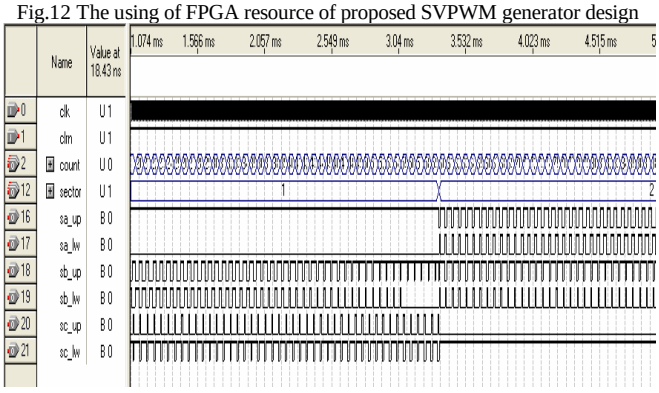
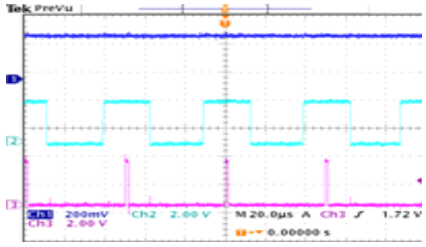
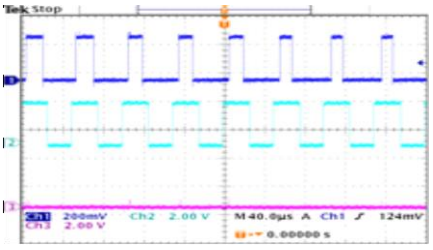


Fig 13. The simulation results of the proposed SVPWM generator

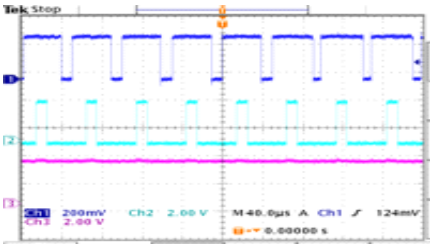
Inherently, Figure 16 shows hardware implementation of proposed SVPWM generator at carrier frequency 20 kHz. The first, second and third channel at Figure 16 (a) and (b) is each S_a, S_b, and S_c switching state respectively, otherwise fourth channel is each (S_a+S_b) line-to-line switching state and its frequency spectrum respectively. The harmonics due to the 20 kHz switching frequency are clearly visible in Figure 16 (b). The similar condition is shown in Figure 17. In this case, carrier frequency is set to 40 kHz; although the testing result as Figure 17 (b) showed that it is detected 38.5 kHz (error 3.75%). These results above have proved that the proposed SVPWM generator has realized in hardware platform based on FPGA and has run with desired.



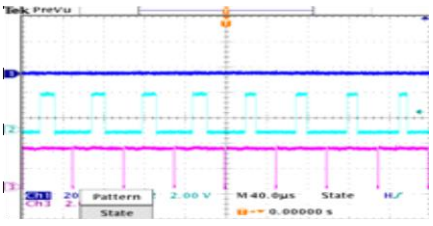
(a) sector 1



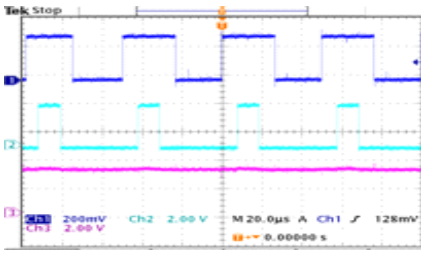
(b) sector 2



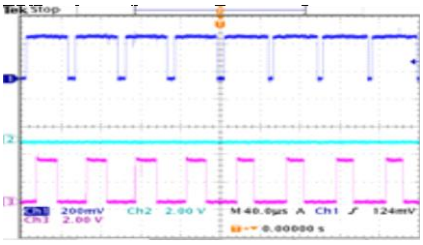
(c) sector 3



(d) sector 4

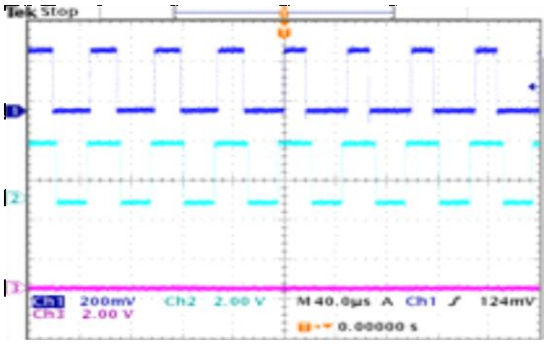


(d) sector 5

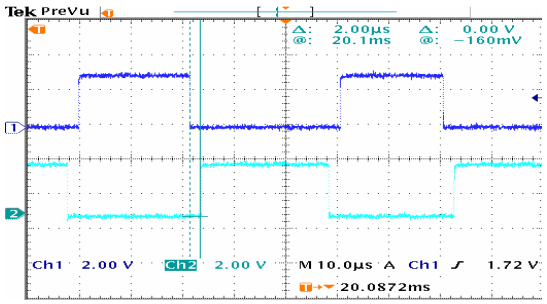


(e) sector 6

Fig.14 The sequence of switching state in each sector

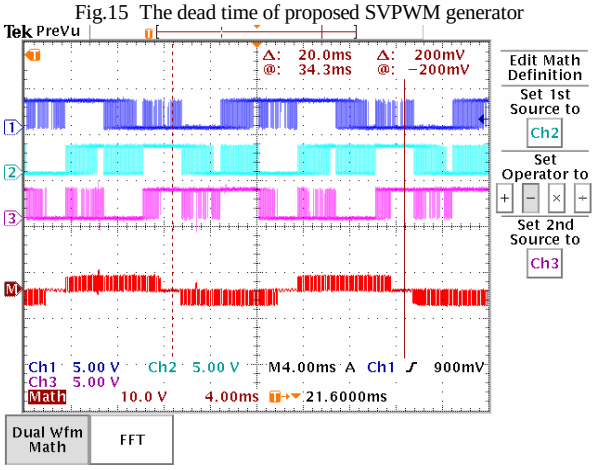


(a) The dead time of S_a switching state in sector 2

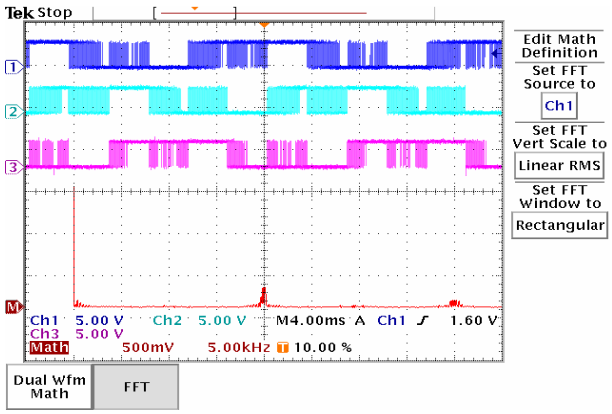


(b) The zoomed dead time of S_a switching state in sector 2

Fig.15 The dead time of proposed SVPWM generator



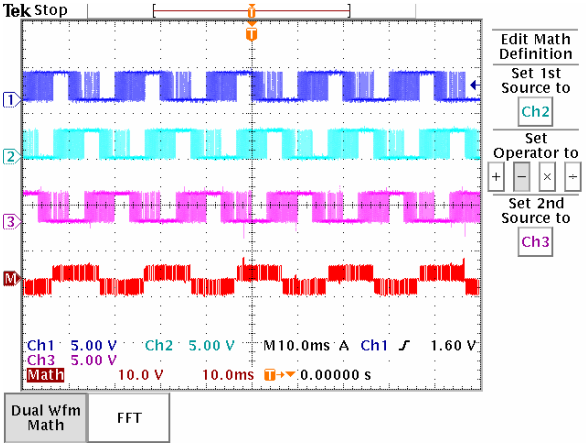
(a) The switching state and its line-to-line



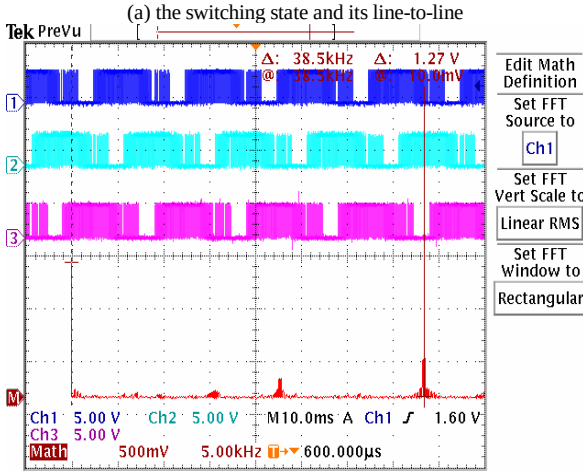
(b) The signal gating and its frequency spectrum

Fig.16 Hardware implementation of proposed SVPWM generator at carrier frequency 20 kHz.

To test the performance of FPGA based proposed SVPWM generator design, this design has been used to drive a three phase inverter system with induction machine 1.5 kW as load. Figure 18 shows the practical result for output stator current (I_a), output phase-to-phase voltage (V_{ab}), frequency spectrum and output voltage line-to-neutral (V_{an}). This figure shows that the practical result obtained from test-rig is in good agreement.



(a) the switching state and its line-to-line



(b) The signal gating and its frequency spectrum

Fig.17 Hardware implementation of proposed SVPWM generator at carrier frequency 40 kHz.

The results above have proved that the proposed SVPWM generator has realized in hardware platform based on FPGA

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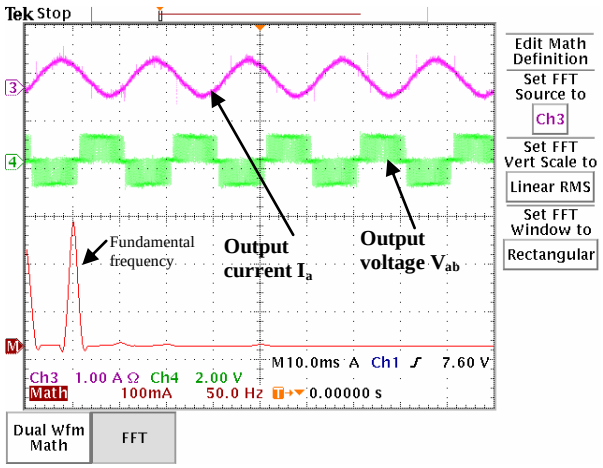
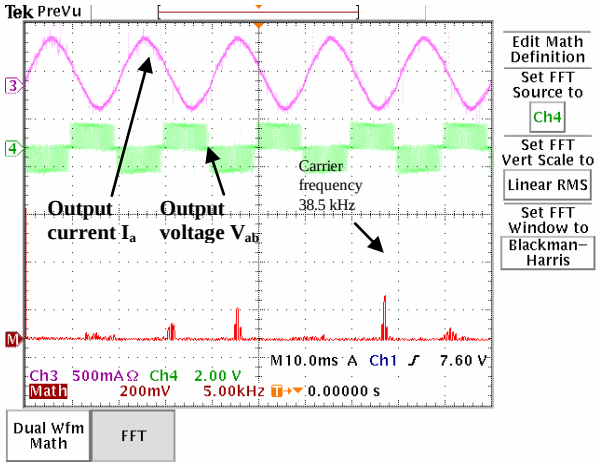
and has run with desired.

VI. Conclusion

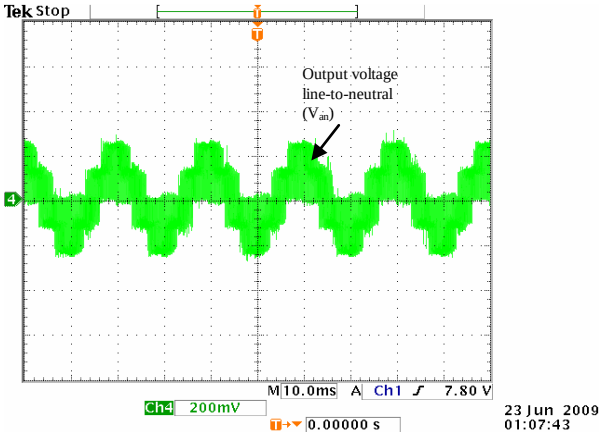
This paper presents the design and simple realization of FPGA based a novel 5-segment discontinuous SVPWM with a difference approach, in which the judging of sectors and the calculation of the firing time to generate the SVPWM waveform is simple, and also the switching losses is low. The proposed SVPWM scheme has been designed and successfully implemented by using APEX20KE Altera FPGA considering hardware-resource saving. It is simple and without compute the angles of each sector to determine number of sector and the commutation pattern and that it has programmed to FPGA successfully in some carrier frequency until 40 kHz. Moreover, this scheme has simple algorithm that it can be implemented easily based on FPGA without computational burden and has successfully driven a three phase inverter system with induction machine 1.5 kW as load.



(a) output current and voltage



(b) frequency spectrum



(c) output voltage line-to-neutral

Fig.18 The performance of FPGA based proposed SVPWM generator design.

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